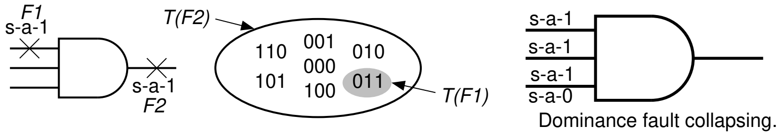

Figure 4.10: An example where fault $F2$ dominates fault $F1$.

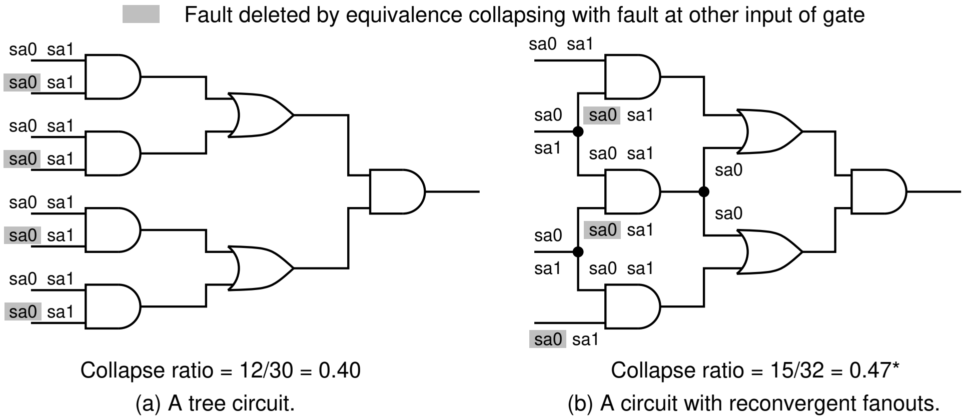

Figure 4.11: Examples of dominance fault collapsing.

(see Figure 4.7), we have moved all faults to inputs. Similar collapsing is possible for all other Boolean gates. Thus we can summarize dominance fault collapsing as:

1. An n-input Boolean gate requires $n + 1$ single stuck-at faults to be modeled.

2. To collapse faults of a gate, all faults from the output can be eliminated retaining one type (s-a-1 for AND and NAND; s-a-0 for OR and NOR) of fault on each input and the other type (s-a-0 for AND and NAND; s-a-1 for OR and NOR) on any one of the inputs.

3. The output faults of the NOT gate, the non-inverting buffer, and the wire can be removed as long as both faults on the input are retained. No collapsing is possible for fanout.

Example 4.12 *Dominance fault collapsing. Figure 4.11 shows the application of the above rules of dominance fault collapsing to the circuits without and with fanouts. Collapsing is done in an output to input pass. A comparison with Figure 4.8 shows the lower collapse ratio for dominance fault collapsing. For the fanout-free circuit, the collapsed fault set only contains input faults. This is an important result. For the circuit with fanouts, the collapsed set contains faults located at "checkpoints" (see Definition 4.7.)*

Theorem 4.1 *Fault detection in fanout-free circuit. A test set that detects all single stuck-at faults on all primary inputs of a fanout-free circuit must detect all single stuck-at faults in that circuit.*

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*Earlier printings gave a ratio $17/32 = 0.53$, obtained by collapsing only among checkpoints.