[35] V. D. Agrawal and H. Kato, "Fault Sampling Revisited," *IEEE Design & Test of Computers*, vol. 7, no. 4, pp. 32–35, Aug. 1990.

[36] V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A Tutorial on Built-In Self-Test, Part 1: Principles," *IEEE Design & Test of Computers*, vol. 10, no. 1, pp. 73–82, Mar. 1993.

[37] V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A Tutorial on Built-In Self-Test, Part 2: Applications," *IEEE Design & Test of Computers*, vol. 10, no. 2, pp. 69–77, June 1993.

[38] V. D. Agrawal and M. R. Mercer, "Testability Measures – What Do They Tell Us?," in *Proc. of the International Test Conf.*, Nov. 1982, pp. 391–396.

[39] V. D. Agrawal and S. C. Seth, *Test Generation for VLSI Chips.* IEEE Computer Society Press, 1988.

[40] V. D. Agrawal, S. C. Seth, and P. Agrawal, "Fault Coverage Requirements in Production Testing of LSI Circuits," *IEEE Journal of Solid-State Circuits*, vol. SC-17, pp. 57–61, Feb. 1982.

[41] A. V. Aho, J. E. Hopcroft, and J. D. Ullman, *The Design and Analysis of Computer Algorithms.* Reading, Massachusetts: Addison-Wesley, 1974.

[42] R. C. Aitken, "Diagnosis of Leakage Faults with $I_{DDQ}$," *Journal of Electronic Testing: Theory and Applications*, vol. 3, no. 4, pp. 367–375, Dec. 1992.

[43] S. B. Akers, "Binary Decision Diagrams," *IEEE Trans. on Computers*, vol. 27, no. 6, pp. 509–516, June 1978.

[44] S. B. Akers, "Functional Testing with Binary Decision Diagrams," in *Proc. of the International Fault-Tolerant Computing Symp.*, June 1978, pp. 82–92.

[45] S. B. Akers, C. Joseph, and B. Krishnamurthy, "On the Role of Independent Fault Sets in the Generation of Minimal Test Sets," in *Proc. of the International Test Conf.*, Sept. 1987, pp. 1100–1107.

[46] W. P. Albrecht Jr., *Microeconomic Principles.* Englewood Cliffs, New Jersey: Prentice-Hall, 1979.

[47] R. W. Allen, C. D. Chen, M. M. Ervin-Willis, K. R. Rahlfs, R. E. Tulloss, and S. L. Wu, "DORA: A System of CAD Post-processors Providing Test Programs and Automatic Diagnostics Data for Digital Device and Board Manufacture," in *Proc. of the International Test Conf.*, Oct. 1981, pp. 555–560.

[48] A. P. Ambler, M. Abadir, and S. Sastry, *Economics of Design and Test for Electronic Circuits and Systems.* Chichester, UK: Ellis Horwood Limited, 1992.

[49] A. P. Ambler, P. Agrawal, and W. R. Moore, editors, *Hardware Accelerators for Electrical CAD.* Bristol: Adam Hilger, 1988.

[50] A. P. Ambler, P. Agrawal, and W. R. Moore, editors, *CAD Accelerators.* Amsterdam: North-Holland, 1991.

[51] A. P. Ambler, M. Paraskeva, D. F. Burrows, W. L. Knight, and I. D. Dear, "Economically Viable Automatic Insertion of Self-Test Features for Custom VLSI," in *Proc. of the International Test Conf.*, Sept. 1986, pp. 232–243.

[52] E. A. Amerasekera and D. S. Campbell, *Failure Mechanisms in Semiconductor Devices.* Chichester, UK: John Wiley & Sons, Inc., 1987.

[53] H. Ando, "Testing VLSI with Random Access Scan," in *Proc. of the COMPCON*, Feb. 1980, pp. 50–52.

[54] J. H. Arabian, *Computer Integrated Electronics Manufacturing and Testing.* New York: Marcel Dekker, 1989.