C.5 Built-In Self-Test

- P. H. Bardell, W. H. McAnney, and J. Savir, *Built-In Test for VLSI: Pseudorandom Techniques*. Somerset, New Jersey: Wiley, 1987.
- S. W. Golomb, *Shift Register Sequences*. Laguna Hills, California: Aegean Park Press, 1982.
- P. Pal Chaudhuri, D. Roy Chowdhury, S. Nandi, S. Chattopadhyay, *Additive Cellular Automata Theory and Applications*. Los Alamitos, California: IEEE Computer Society Press, 1997.
- S. Pilarski and T. Kameda, *A Probabilistic Analysis of Test-Response Compaction*. Boston: Kluwer Academic Publishers, 1995.
- J. Rajski and J. Tyszer, *Arithmetic Built-In Self-Test for Embedded Systems*. Englewood Cliffs, New Jersey: PTR Prentice Hall, 1998.
- C. E. Stroud, *A Designer's Guide to Built-In Self-Test*. Boston: Kluwer Academic Publishers, 2002.
- C. Ronse, *Feedback Shift Registers*. Berlin: Springer-Verlag, 1984.
- V. N. Yarmolik and S. N. Demidenko, *Generation and Application of Pseudorandom Sequences for Random Testing*. Chichester, United Kingdom: John Wiley & Sons, 1988.
- V. N. Yarmolik and I. V. Kachan, *Self Testing VLSI Design*. Amsterdam, The Netherlands: Elsevier, 1993.

C.6 Delay Fault Test

- A. Krstić and K.-T. Cheng, *Delay Fault Testing for VLSI Circuits*. Boston: Kluwer Academic Publishers, 1998.
- M. Sivaraman and A. J. Strojwas, *A Unified Approach for Timing Verification and Delay Fault Testing*. Boston: Kluwer Academic Publishers, 1998.

C.7 Design for Testability

- V. D. Agrawal, editor, *Special Issue on Partial Scan Methods*, volume 7 of *Journal of Electronic Testing: Theory and Applications*. Boston: Kluwer Academic Publishers, August-October 1995.
- F. P. M. Beenker, R. G. Bennetts, and A. P. Thijssen, *Testability Concepts for Digital ICs: The Macro Test Approach*. Boston: Kluwer Academic Publishers, 1995.
- R. G. Bennets, *Design of Testable Logic Circuits*. Reading, Massachusetts: Addison-Wesley, 1984.
- A. L. Crouch, *Design-for-Test for Digital ICs and Embedded Core System*, Piscataway, New Jersey: IEEE Press, 2000. *Co-published with Prentice Hall PTR.*
- E. B. Eichelberger, E. Lindbloom, J. A. Waicukauski, and T. W. Williams, *Structured Logic Testing*. Upper Saddle River, New Jersey: Prentice-Hall, 1991.
- W. M. Needham, *Designer's Guide to Testable ASIC Devices*. New York: Van Nostrand Reinhold, 1991.
- C. C. Timoc, *Selected Reprints on Logic Design for Testability*. Los Alamitos, California: IEEE Computer Society Press, 1984.
- F. F. Tsui, *LSI-VLSI Testability Design*. New York: McGraw-Hill, 1986.
- J. Turino, *Design to Test*. Florence, Kentucky: Van Nostrand Reinhold, 1990.