is now done with silicon devices in the chip, rather than with external reed relays and wire. This introduces additional, unwanted impedances during testing, and additional current leakage paths to ground. Table 17.1 [511] shows how silicon switches are less desirable than the conventional reed-relay switches in the analog ATE. Notice how the CMOS switch of the 1149.4 standard has an on-resistance four or more decades higher than a reed relay, but is 4 million times smaller and hundreds of times faster. Also, the CMOS switch is somewhat non-linear over larger signal swings. These effects must be accounted for when using the 1149.4 bus, or inaccurate test measurements will be made. Figure 17.3 [511] shows how linear ICs can be chained along the 1149.4 test bus. Lofstrom [504] states that 1149.4 will not be used for directly measuring the quality of a signal, because switches are too slow and non-linear. The 1149.4 bus is slow, and usually has less than 1 MHz bandwidth. Components are usually tested with 10 $kHz \leq f \leq 100$ kHz, but these frequencies are still adequate for measuring very small capacitances and inductances [504]. One needs to limit the number of analog measurements, possibly by using the pseudo-1149.1 test on analog pins to check for shorts and opens, because accurate current and voltage measurements are slow (many ms per reading) and therefore expensive [504]. The pseudo test switches the pin between V_H and V_L, and uses the digitizing receiver at the other end of the interconnect (driven by the pin) to check the interconnect for shorts and opens.

Table 17.1: Switches in various technologies.

Parameter	Mechanical relay (surface mount)	CMOS switch ($0.35\ \mu m$)	Bipolar switch ($0.35\ \mu m$)
On-resistance	$10^{-2}\ \Omega$	10^2 to $10^3\ \Omega$	Varies
Off-resistance	$10^{12}\ \Omega$	$10^{12}\ \Omega$	$10^{10}\ \Omega$
Bidirectional?	Yes	Yes	No
Switching time	$\geq 500\ \mu s$	$< 1\ \mu s$	$< 1\ \mu s$
Area	$96.7 \times 10^6\ \mu m^2$	$20\ \mu m^2$	100 to $5000\ \mu m^2$

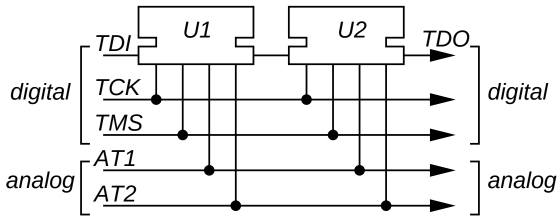

Figure 17.3: Chaining of 1149.4 ICs.

17.2.2 Analog Test Access Port (ATAP)

The *analog test access port* (ATAP) has four required and one optional signals from the 1149.1 digital boundary scan standard (see Chapter 16.) These signals