Each output requires two test patterns for a sa0 and a sa1 test. Each interconnect is sampled during testing by all chips that receive the signal. During interconnect test, all output pins on the chip driving the interconnect will be enabled, and all input pins on all other chips must latch the signal. Describe the JTAG instruction sequence needed to test the interconnect, and calculate the test time at a 100 MHz clock rate.

16.5 *Interconnect delay test time.* Use the same system of Problem 16.4, but now compute the test modes and test time to perform interconnect delay fault test. This requires, for each interconnect being tested, a two-pattern test for a rising transition, and another for a falling transition delay test. Describe the JTAG instruction sequence needed to test the interconnect, and calculate the test time at a 100 MHz clock rate.

16.6 *Boundary scan delay fault test.* Figure 16.17 shows two boundary scan cells surrounding the on-chip system logic. We test the path from the INPUT boundary scan cell, through the on-chip system logic, and ending at the OUTPUT boundary scan cell. The JTAG commands are: *SAMPLE*, *PRELOAD*, *EXTEST*, *INTEST*, *RUNBIST*, *CLAMP*, *IDCODE*, *USERCODE*, *HIGHZ*, and *BYPASS*. Please explain the sequence of these commands used for delay fault testing of this particular path.

16.7 *Test controller.* Implement a logic-level finite state machine realizing the test controller state diagram in Figure 16.11. The controller has output active high signals indicating when it is in the state *Shift-DR*, *Shift-IR*, *Update-DR*, *Update-IR*, *Capture-DR*, *Capture-IR*, *Run-Test/Idle*, or *Test-Logic-Reset*. These signals control the boundary scan register. If a sequential automatic test-pattern generator is available, generate tests for your test controller and determine whether the controller itself is testable.

16.8 *Bus and controller testing.* In Figure 16.32, the three memory chips are pretested. However, 512 patterns must be applied by an external tester to the *System Logic 1* chip. Describe the test instructions, configurations, and procedures for the *System Logic 1* and *2* chips for stuck-fault testing of the *System Logic 1* chip, without burning out the *Bus* or Memory chips. Calculate the test time with a clock rate of 100 MHz and an external tester. Now, describe a test configuration and procedure to test the wires from the *System Logic 1* chip to each memory chip, and to test the Bus between the memory chips and the *System Logic 2* chip, under the same test conditions.

16.9 *Memory testing.* Test a 1 *Gb* DRAM using boundary scan, the MARCH C– test (see Chapter 9), and an external tester. The chip has these signals:

Signal	# Bits	Signal	# Bits
CS	1	Address	28
$R/\overline{W}$	1	Data	4