The function $1 - Y(T)$ is called the *fallout rate*. It is an important relation that will be used in the next subsection for obtaining the yield parameters, f and β, from the chip test data. The true process yield is obtained by substituting $T = 1$, as

$$Y = Y(1) = [1 + Af/\beta]^{-\beta} \tag{3.19}$$

When chip tests have a fault coverage T, the defect level is given by

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)} = 1 - \frac{Y(1)}{Y(T)} = 1 - \left(\frac{\beta + TAf}{\beta + Af}\right)^{\beta} \tag{3.20}$$

This equation gives DL as a fraction that should be multiplied by 10^6 to obtain *parts per million* (*ppm*.) We can verify that for zero fault coverage, $DL(0) = 1 - Y(1)$, where $Y(1)$ is the process yield. For a 100% fault coverage, $DL(1) = 0$.

3.3.2 Defect Level Estimation

We will apply the preceding analysis to assess the defect level of a chip designed and tested at IBM under a SEMATECH experiment on test methods [501]. It is a bus interface controller ASIC chip containing 116,000 equivalent (two-input NAND) gates. It has 249 I/O signals and a 304-pin package. Some portions of the chip operate at a 40 MHz clock and others at 50 MHz. There are 5,280 scan latches (full-scan.) The chip operates with a 3.3 V supply. The die size is 9.4 $mm \times 8.8$ mm. It was fabricated using a $0.8 \mu m$ CMOS process* with three levels of metal.

Although four types of tests (stuck-at, functional, delay, and I_{DDQ}) were used to test the device, our analysis is based on stuck-at fault tests applied at the wafer level. The chip was designed in IBM's *level-sensitive scan design* (LSSD) style, which allows a scan flush test (see Chapter 14.) In this test, all flip-flops form a chain and both master and slave clocks are turned on, simultaneously. Signal transitions propagating through the long uninterrupted path test timing and many other faults. With additional scan tests, the total stuck-at fault coverage was 99.79% over a total of 375,142 faults. The fault coverage, as determined by a fault simulator, is shown in Figure 3.5 as a fraction instead of percentage.

Wafers were tested on an Advantest 3381 ATE, which applied vectors at 2.5 MHz. The cumulative chip fallout (fraction of chips failing up to a vector in the test set) is shown in Figure 3.6. This graph was obtained from the wafer level test of 18,466 chips. The fallout fraction rises to 0.2386 because the yield is near 76%. The two sets of data show similarity. As the fault coverage rises, more faulty chips fallout. That is all we can tell from these graphs. However, we would like to know how many bad chips are still in the "good" lot when the testing stops. That precisely is the question that the defect level answers.

A sample of the raw fault simulator and chip test data is shown in Table 3.2. The second and third columns of this table list the number of faults detected and the number of chips failing by the vector whose sequence number appears in the first column. The last two columns show the normalized cumulative data that are

*Incorrectly reported as $0.45 \mu m$ in previous printings.