circuit and then generate tests. Recent variations of the technique are partial-scan and boundary scan. In general, partial-scan requires the use of sequential ATPG. However, there are partial-scan techniques that use combinational ATPG. Such techniques either assume unknown states for unscanned flip-flops [32], or make the circuit "completely" acyclic by removing even the self-loops [274, 379]. In either case, the scan percentage can be 50% or higher.

A scan overhead of about 10 to 15% is generally considered acceptable in ASIC chips. In addition, there may be a speed penalty, which can be less than 5%. These costs are justified by the high quality of devices obtained in a short design time.

Problems

14.1 *Importance of initialization.* The circuit in Figure 14.15 produces a toggling output when the input is 1. Input 0 holds the output at 0. Assuming the state of the flip-flop (FF) to be unknown, derive a test for the s-a-1 fault shown. Explain why this fault is only potentially detectable. What design change is needed to make the test deterministic?

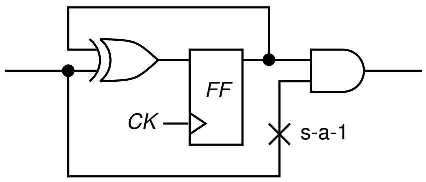

Figure 14.15: A toggle circuit.

14.2 *MUX design.* Design an economical static CMOS two-to-one multiplexer.

14.3 *Multiple scan chains.* Rederive Equations 14.1 and 14.2 when flip-flops are distributed in n_{chain} scan chains of equal length. Assume that only one extra pin is available for test, but the number of primary input and output data pins is not limited.

14.4 *Scan tests.* Suppose that your chip has 100,000 gates and 2,000 flip-flops. A combinational ATPG program produced 500 vectors to fully test the logic. According to Section 14.2.2, a single scan-chain design will require about 10^6 clock cycles for testing. Find the scan test length if 20 scan chains are implemented. Given that the circuit has 20 primary input and 20 primary output data pins, and only one extra pin can be added for test, how much more gate overhead will be needed for the new design?

14.5 *Modulo-5 counter.* To repeat Example 14.1 design a modulo-5 counter circuit that counts from 0 to 4 and then resets to 0. A single output becomes 1 only when the count is 4. Using an ATPG program make the combinational logic irredundant and then find any untestable faults in the sequential circuit.