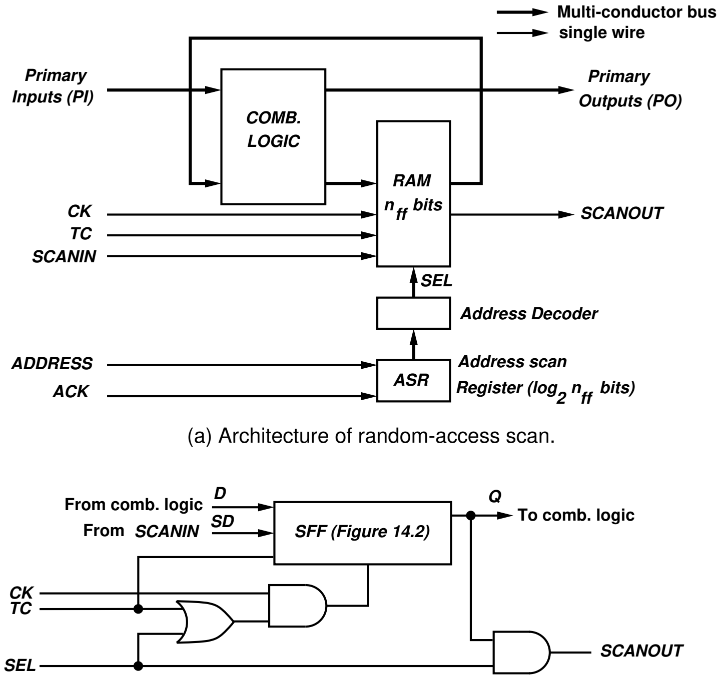

(a) Architecture of random-access scan.

(b) A flip-flop for random-access scan*.

Figure 14.14: Random-access scan (RAS.)

the state of SD is latched in that flip-flop by the clock CK. The SD inputs of all flip-flops in RAM are tied together to the $SCANIN$ pin. However, the $SCANIN$ signal is not latched in the unaddressed flip-flops because $SEL = 0$ inhibits the clock CK.

The ability to control and observe individual flip-flops has the advantage of reducing the length of the test sequence. RAS has been used in practice [53], but has not gained popularity perhaps due to a large overhead. First the *scan flip-flop* (SFF) requires additional logic shown in Figure 14.14(b). Then, an address decoder and *address scan register* (ASR) are added. The routing of SEL signals, if flip-flops are distributed over a VLSI chip, can also take a significant amount of area.

Despite its drawbacks, the RAS technique may have benefits in partial-scan where only a few flip-flops need scanning, or in delay testing where a change of single flip-flop states can provide good tests [371].

14.5 Summary

Scan design has been the backbone of design for testability in the industry for about three decades. It continues to be the most popular technique. It is often supported by design automation tools that can insert scan logic into a predesigned

*Simplified circuit after removing a redundant gate from the version that appeared in earlier printings (2000 and 2001), as observed by Prof. S. Seth of University of Nebraska.