application of a vector-pair (V_1, V_2) is as follows:

1. Set $HOLD = 0$ and $TC = 0$, and scan the state variable bits of V_1 into the scan register using the clock CK.

2. Set $TC = 1$.

3. Set $HOLD = 1$ and apply the primary input portion of V_1. Thus the entire vector V_1 appears at the inputs of the combinational logic.

4. Change $HOLD$ to 0.

5. Repeat Steps 1, 2, and 3 for V_2. This produces a $V_1 \rightarrow V_2$ transition at the inputs of the combinational logic.

6. Change $HOLD$ to 0, and capture the output of the combinational logic in SFF by applying the clock CK.

7. Set $TC = 0$ and apply clocks to scan out the contents of flip-flops. This completes the application of one vector-pair delay test.

In general, delay tests will contain several vector-pairs. The scanout following the second vector of one pair can be overlapped with the scanin of the first vector of the next pair.

The hardware overhead of a SHFF consists of the hold latch, which increases the size of the scan flip-flops by about 30%. One extra input pin is needed for the $HOLD$ signal, which must be routed to all flip-flops. The technique also has a performance overhead. Although hold latches remain transparent in the normal operation ($HOLD = 1$) of the circuit, they add 1 to 2 gate delays in signal paths. Despite these penalties, the SHFF offers a feasible DFT discipline for delay testing.

Random-Access Scan (RAS.) In this technique, the scan function is implemented like a random-access memory (RAM) [7, 721, 724]. A general architecture is given in Figure 14.14(a). Here all flip-flops form a RAM in the scan mode. In general, a subset of flip-flops can be included in the RAM if partial-scan is desired. In the normal mode ($TC = 1$), all flip-flops receive data from the combinational logic under the control of the clock CK. Flip-flop outputs directly feed into the combinational logic. A typical design of a cell in this RAM is given in Figure 14.14(b). In the scan mode, this scheme allows reading or writing of any selected flip-flop. The flip-flop address, which may contain $log_2 n_{ff}$ bits when there are n_{ff} flip-flops in the RAM, is serially loaded into an *address scan register* (ASR) using an address clock ACK. The address decoder now produces the select signal $SEL = 1$ for the addressed flip-flop. The SEL signals to all other flip-flops remain 0. The $SCANOUT$ signals of all flip-flops are tied into an OR-bus feeding the $SCANOUT$ pin. Thus, the content of the addressed flip-flop appears at this output. An advantage of this method is that any flip-flop can be observed even when the circuit is in the normal mode ($TC = 1$.)

For scanning data into a flip-flop, the scan mode ($TC = 0$) is used. Assuming that the select signal ($SEL = 1$) has been generated for the addressed flip-flop,