as parts per million (*ppm.*) Other terms used for defect level are *reject ratio* and *field reject rate.*

The defect level is determined from the field return data. After VLSI chips leave the manufacturing facility, they may fail and be returned to the manufacturer (for a possible refund!) Some possible ways are listed below:

- *Failing acceptance test.* The customer (or user) conducts an *acceptance test* on the parts before they are mounted on printed circuit boards. If a part fails the test it is returned to the supplier.

- *Failing system test.* A board fails the *system test* but passes when one or more chips are replaced. The removed chips are returned to the chip supplier.

- *Failing maintenance test.* A *maintenance test* is conducted on a system operating in the field (usually on site) for both regular maintenance and diagnosis when an operational failure occurs. The faulty part, e.g., a board, is located and replaced. While the system goes back to operation, the replaced board is returned to a repair shop, where faulty chips are found and replaced. The faulty chips are returned to the chip supplier.

The chips thus returned are examined by the manufacturer to determine the causes of failures. These causes may point to areas of improvement in specification, design, fabrication or test. Such improvements reduce the defect level. For VLSI chips, while a defect level of 500 *ppm* may be acceptable, 100 *ppm* or lower represents high quality.

3.3.1 Test Data Analysis

The above procedure of finding the defect level has several problems. First, not all failing parts are generally returned. Second, some returned parts are damaged due to mishandling or improper use and their cause of failure may be incorrectly diagnosed. Third, it takes a long time (usually a year or more) to collect sufficient data even on high-volume (million chips per year) parts. And fourth, as improvements are made the defect level reduces over time and, therefore, a time averaging of the number of returned parts gives an overly pessimistic defect level, especially for the early part of production and for low-volume production. The following technique of test data analysis provides an assessment of the defect level from the test data analysis of the manufacturing test. Although the field data is essential in the long run, the analysis helps the chip manufacturer to assess and improve the quality before the chips are supplied to the user.

Defects versus faults. We defined defects in the first paragraph of Section 3.2 as physical imperfections. The term *fault* is used to refer to electrical, Boolean, or functional malfunctions. In general, a physical defect in a chip can produce multiple faults. Thus, the spatial distribution of faults on a wafer is also clustered, sometimes even more so than the defects. We will rederive yield expressions for fault density. This will provide a relationship between the test process and yield and allow us to