where $\Gamma(x)$ is the Gamma function, defined as [715]:

$$\Gamma(x) = \int_0^\infty e^{-y} y^{x-1} dy$$

The mean, $E(x)$, and variance, $\sigma^2(x)$, of x are given by:

$$E(x) = Ad \tag{3.10}$$

$$\sigma^2(x) = Ad(1 + Ad/\alpha) \tag{3.11}$$

The values of $E(x)$ and $\sigma^2(x)$ for the number of defects on a chip are obtained either from experimental measurements or by process simulation [167, 710]. Substitution in the above equations then leads to the determination of yield parameters, d and α. The yield is obtained as the probability, $p(0)$, of no defect on a chip. Thus, substituting $x = 0$ in Equation 3.9, we get:

$$Y = (1 + Ad/\alpha)^{-\alpha} \tag{3.12}$$

When $\alpha \to \infty$, Equation 3.9 gives the *Poisson density function* with mean Ad, which corresponds to the unclustered distribution of defects (Figure 3.4(a)):

$$\text{For unclustered defects:} \quad p(x) = \frac{(Ad)^x e^{-Ad}}{x!} \tag{3.13}$$

On substituting $x = 0$ this gives the yield, which can also be obtained by substituting $\alpha = \infty$ in Equation 3.12, as

$$Y_{\text{Poisson}} = e^{-Ad} \tag{3.14}$$

Equation 3.14 gives very low yields. For example, if the average number of defects is $Ad = 1.0$ and $\alpha = 0.5$, which are quite typical for a large VLSI chip, then $Y_{\text{Poisson}} = 1/e = 0.37$. A yield of 37% is considered to be too low for a profitable manufacturing. A more realistic yield, which characterizes a mature process, is obtained from Equation 3.12 as 58%.

When the processing of a newly designed chip is first started, the yield may be low. It may even conform to the prediction of Equation 3.14. The diagnosis of defects leads to process improvements to a stage where no further improvement is possible. The resulting process, called *matured*, has significantly higher yield as compared to the new process yield.

Example 3.5 *Cost of testability overhead. Consider a VLSI manufacturing process characterized by: defect density, $d = 1.25$ $defects/cm^2$, and clustering parameter, $\alpha = 0.5$. The area of a chip is $A = 8\ mm \times 8\ mm = 0.64\ cm^2$. Equation 3.12 gives the yield as:*

$$Y = \left(1 + \frac{0.64 \times 1.25}{0.5}\right)^{-0.5} = 0.62$$