hard faults, which cause field failures. Mao and Gulati selected test vectors for single leakage faults [428] so that they also cover multiple leakage faults.

Weak Faults. An n MOSFET cannot pass logic 1 (traditionally 5 V) without degrading it to 5 $V - V_{tn}$. Similarly, a p MOSFET cannot pass logic 0 (0 V) without degrading it to $|V_{tp}|$. In the CMOS C-switch device, an nFET and a pFET are connected in parallel. A *weak fault* causes one of the devices to fail to turn on, so the signal passed from the source to the drain of the C-switch is degraded (has a *weak* voltage), which increases propagation delays and increases noise [428]. A path between the n_i and n_j nodes is a *transmission path* if a chain of channel connected transistors exists between n_i and n_j. Channel connected means that all of the channels of the transistors could be shorted together if all transistors were turned on. In a *conducting path* all transistors in a transmission path are turned on. A *normal-1 (0) transmission path* has only pMOS (nMOS) transistors. A path with at least one pMOS (nMOS) transistor is a *weak-0 (1) transmission path.* Similarly, we define *normal-1 (0) conducting paths* and *weak-0 (1) conducting paths.*

Figure 13.6 shows transistors *N4* and *N5* forming a normal-0 transmission path from V_{SS} to node A [428]. *P2* and *P3* form a normal-1 transmission path from V_{DD} to *O1*. When (*I1*, *I2*)$=(1,0)$, *P2* and *P3* form a normal-1 conducting path, and *P2* and *N3* form a weak-1 conducting path, from V_{DD} to *O1*.

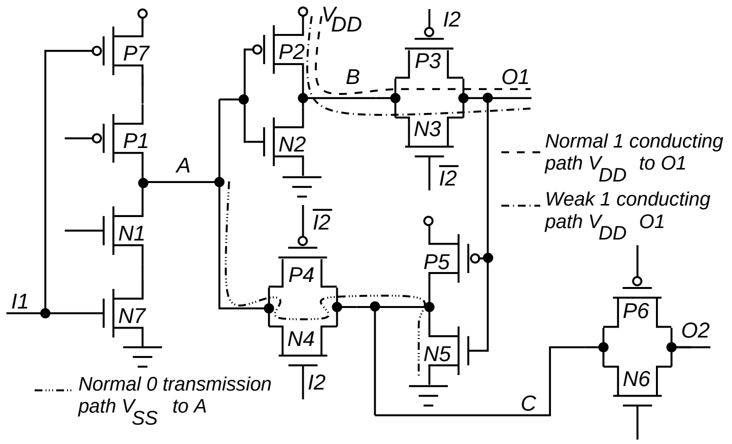

Figure 13.6: Circuit with transmission, normal, and weak conducting paths.

There are two *necessary* and *sufficient* conditions to have a weak-0 (1) fault [428]. There must be at least one normal-0 (1) conducting path between n_i and V_{SS} (V_{DD}) in the good circuit, and all normal-0 (1) conducting paths should be blocked in the bad circuit. There must be at least one weak-0 (1) conducting path between node n_i and V_{SS} (V_{DD}) in the bad circuit [272]. A node may have multiple weak-0 (1) faults, which must be considered separately because detection of one does not imply detection of the others. We assume that a weak-0 (1) fault at a node is caused by blocking of all normal-0 (1) conducting paths due to a single defective transistor.