Figure 13.5 shows the I_{DDQ} dependence on K and R_b (bridging resistance in S_1) values. For the small R_b range, the I_{DDQR_b} dependence on the relative size is high because I_{DDQR_b} values directly depend on the resistance offered by the transistor in the conducting path. There is also an I_{DDQR_b} dependence when $R_b > 50\ K\Omega$. For $0 \leq R_b \leq 100\ K\Omega$ the I_{DDQR_b} current changes from $2\ \mu A$ to $50\ \mu A$, so bridges exhibit good current testability. Below the critical resistance, the circuit is voltage and current testable. Above the critical resistance, the circuit is only current testable or delay fault testable. The largest I_{DDQR_b} deviation is when V_{IN} is $0\ V$, because the bridged nodes have opposite logic values. The maximum I_{DDQ} current occurred when $R_b = 3.5\ K\Omega$, because of the current contribution of the non-defective inverter stages [580]. A maximum deviation of 8.5% of the total I_{DDQ} current happened for low resistive shorts. For high resistive shorts, the agreement was excellent for all bridging faults in the inverter chain with deviations below 0.1%.

CMOS Stuck-Open Faults. CMOS transistors stuck-open cause high impedance states at a logic gate output, and under certain situations, I_{DDQ} is elevated and the fault can be detected [617]. I_{DDQ} testing does not guarantee detection, but works in practice [618] because the floating output node is capacitively coupled into the substrate, as well. The coupling often results in an intermediate voltage on the node [332, 616]. Mao and Gulati select I_{DDQ} vectors for testing the case of transmission gates driving multi-input logic gates [428].

Delay Faults. Most random CMOS defects cause a timing delay fault, rather than a catastrophic failure [332, 614, 616]. Many of these defects elevate I_{DDQ} current, which also changes the signal rise and fall times [617]. Many delay faults are detected with few I_{DDQ} test vectors. However, there is a defect subset that causes a delay fault, but does not elevate I_{DDQ} current, by increasing interconnect resistance at vias, or by increasing the transistor threshold voltage [614]. Motorola used I_{DDQ} tests to detect delay faults [271]. Metal briding shorts in 256 K SRAMs caused a $3\ ns$ increase in data path delay, and increased the I_{DDQ} current 2 to 3 times. I_{DDQ} testing may be an inexpensive way to detect some delay faults.

Leakage Faults. Mao and Gulati [428] developed the *leakage fault* model, which accounts for leaking current between the *gate*, *source*, *drain*, or *bulk* terminals of a MOSFET. There should be no leakage in a healthy MOSFET, except between source and bulk and also between drain and bulk, and this must be less than a specified value. Gate oxide shorts can cause leakage between gate and source or between gate and drain. They proposed these six leakage faults for each MOSFET:

f_{GS}	– between gate and source	f_{BS}	– between bulk and source
f_{GD}	– between gate and drain	f_{BD}	– between bulk and drain
f_{SD}	– between source and drain	f_{BG}	– between bulk and gate

They assume that the leakage faults do not change circuit logic values, which is true for gate oxide shorts during production test. However, these shorts later develop