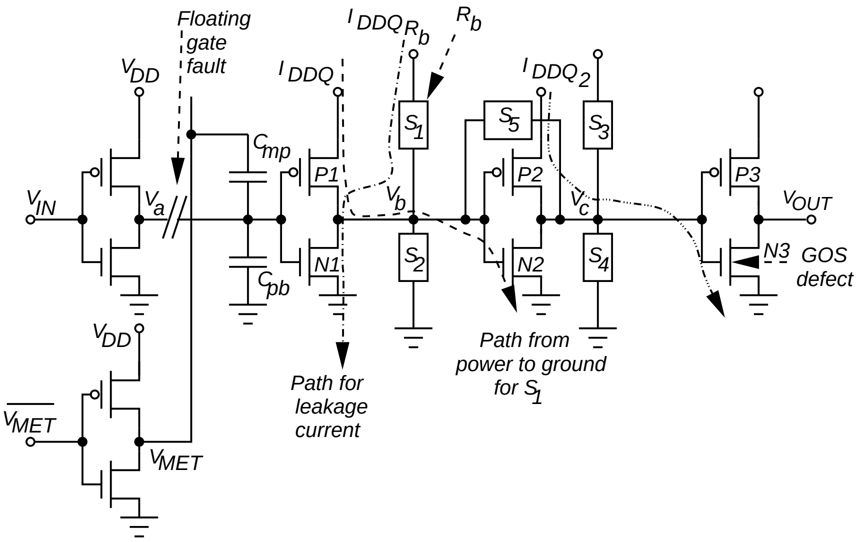

Figure 13.3: Circuit illustrating floating gate, GOS, leakage, and bridging faults.

tunneling [290]. This causes a delay fault, and elevation of I_{DDQ} current, which can be tested with an I_{DDQ} test. A large open results in a stuck-at fault, which sometimes can be tested by an I_{DDQ} test. In Figure 13.2, the open leaves V_{fn} at a voltage that is a function of the circuit parasitics. The output then may behave as a stuck-at fault, and may have either a weak or strong logic voltage because of the logic gate analog voltage gain. A weak output voltage happens when $V_{tn} < V_{fn} < V_{DD} - |V_{tp}|$, and is detected by an I_{DDQ} measurement. If $V_{fn} < V_{tn}$ or $V_{fn} > V_{DD} - |V_{tp}|$, then a stuck-at fault occurs, which is probably not detected by an I_{DDQ} current test, and must be detected by a voltage test, instead.

When large line breaks occur, tunneling effects are negligible. The floating gate voltage is determined by capacitive coupling of the broken polysilicon path to the metal lines crossing it. For certain floating gate defects, the transistor conducts, and for others it remains stuck-open [135, 138, 422]. Figure 13.3 [579, 580] shows the circuit schematic modeling the severed transistor gate with C_{pb}, the capacitance from poly to bulk, and C_{mp}, the overlapped metal wire to floating poly capacitance. The floating gate voltage depends on these capacitances and node voltages. If the nFET gets enough voltage at its gate to turn it on, then a path from V_{DD} to ground exists if the pFET is on, so the abnormal I_{DDQ} current can be sensed. The floating gate voltage is sufficient to activate the faulty transistor over many conditions [579, 580]. Segura *et al.* fabricated five defective inverter chains with deliberate defects causing a floating gate on a 2 μm n-well CMOS process. Here, $1.95\ fF \leq C_{pb} \leq 5.3\ fF$ and $1.1\ fF \leq C_{mp} \leq 5.4\ fF$. Figure 13.4 [580] shows the static transfer characteristics of the five defective circuits. When the pFET gate nears $0\ V$, and the defective nFET is influenced by an overlapping metal track at $5\ V$, I_{DDQ} current testing detects the fault. If the metal were at $0\ V$, I_{DDQ} testing would not work.