12.2 Path-Delay Test

The path-delay fault is an important fault model used in delay testing. The following definitions characterize it.

Definition 12.1 *Path-delay fault. The delay defect in the circuit is assumed to cause the cumulative delay of a combinational path to exceed some specified duration. The combinational path begins at a primary input or a clocked flip-flop, contains a connected chain of gates, and ends at a primary output or a clocked flip-flop. The specified time duration can be the duration of the clock period (or phase), or the vector period. The propagation delay is the time that a signal event (transition) takes to traverse the path. Both switching delays of devices and transport delays of interconnects on the path contribute to the propagation delay.*

For each combinational path in a circuit, there are two path-delay faults corresponding to rising and falling transitions, respectively. These faults for a path consisting of gates a, b, and c are specified as $\uparrow a - b - c$ and $\downarrow a - b - c$, where the arrow gives the direction of the transition at the input of the path. The total number of path-delay faults is twice the number of physical paths in the circuit. In general, any combination of paths can be faulty. However, similar to the "single stuck-at" fault model (see Section 4.5) we consider delay faults of single paths. In practice, though, multiple paths can be faulty.

Definition 12.2 *Non-robust path-delay test. A test that guarantees to detect a path-delay fault, when no other path-delay fault is present, is called a non-robust test for that path. A path-delay fault for which a non-robust test exists is called a "singly-testable path-delay fault [245]."*

A non-robust path delay test applies a transition (two-vectors) at the input of the path and measures the output value after a specified interval (clock period.) For the test to be an effective measure of the path delay, the "expected or correct" output value must be uniquely controlled by the transition propagating through the path. Consider the path-delay fault $\downarrow P3$ shown with bold lines in Figure 12.2. Signals B, E, G, J, and K are called the *on-path signals*. Signals that are not in the path $P3$ but feed the gates on the path are called *off-path signals*. Thus, C and H are off-path signals for $P3$. A non-robust test consists of a vector-pair $V1, V2$, such that:

1. The change $V1 \rightarrow V2$ initiates the appropriate transition at the beginning of the path under test. For example, in Figure 12.2 the vector-pair $(V1, V2) = (010, 100)$ produces a falling transition at B to test the fault $\downarrow P3$.

2. All off-path input signals for the path under test assume non-controlling values (0 when feeding into OR/NOR gate, and 1, into AND/NAND gate) in the steady-state following the application of the second vector $V2$. This condition is known as *static sensitization* of a path. We may point out that the static sensitization of paths should not be confused with the "static timing analysis,"