when they match. A set of semaphore latches controls which port gets *read* and which port gets *write* access when the two ports are in contention (access the same RAM address.) The contention circuit sets the semaphores, and arbitration depends only on relative signal timings.

1. Contention testing [535]. Each chip has a timing parameter called the *arbitration priority set-up time* (T_{aps}), which is the minimum time that the address applied to one port must be stable before the same address arrives at the other port, in order for the first to receive priority. The contention test must ensure that $T_{aps} = 5\ ns$. If the tester has separate X and Y timing generators, this can be guaranteed. Otherwise, we must use address formatting (see Figure 9.35 [442, 535].) We disable the Y-complementer exactly when the address has stopped arriving, so that the Y address leads the X address by T_{aps}.

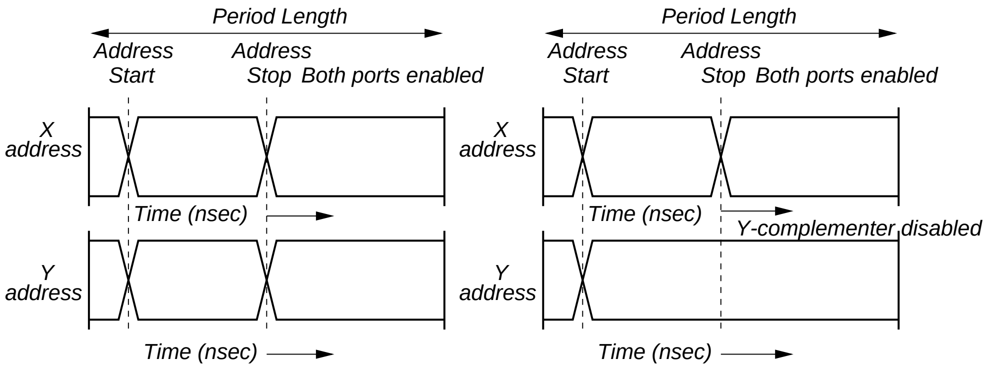

Figure 9.35: X/Y port separation for dual-port RAM testing.

2. Semaphore testing.

	Method:
1.	For each port, request, verify, and release each semaphore latch.

9.8 Summary

No single type of test (march, NPSF, DC parametric, AC parametric) is sufficient for current RAM testing needs, so a combination of various tests is used. Also, *inductive fault analysis* is now necessary, to ensure that the actual defects that are occurring are mapped into a fault model, and then appropriate tests can be selected for that fault model. A reader interested in testing of word-oriented memories may refer to the Appendix C in van de Goor's book [688] for a brief discussion, or to the recent literature[§] for details.

[§]A. J. van de Goor and I. B. S. Tlili, "March Tests for Word-Oriented Memories," *Proc. Design Automation and Test in Europe (DATE) Conf.*, Feb. 1998, pp. 501-508; and I. B. S. Tlili and A. J. van de Goor, *Tests for Word-Oriented Memories*, Report No. 1-68340-44(1977)08, Delft University of Technology, Dept. of Electrical Eng., Delft, The Netherlands.