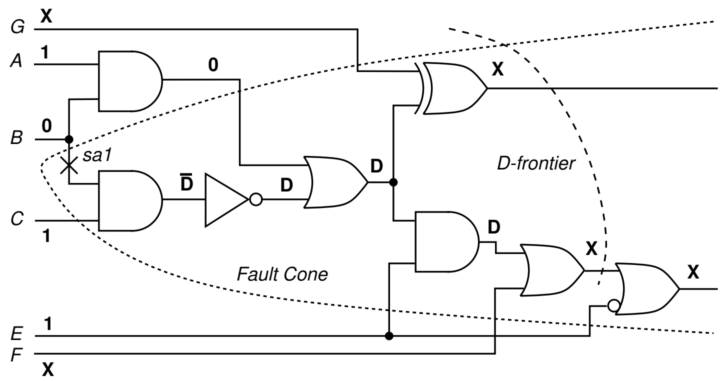

Figure 7.12: Fault cone.

that one may have to use extra logic to have an optimum-speed irredundant circuit. Gharaybeh *et al.* [244] report that they had to add as many as 41% more gates to obtain an irredundant delay-optimized design of the benchmark circuit s1238.

7.3 Testing as a Global Problem

Figure 7.11 shows two sub-assemblies A and B. By itself each sub-assembly is fully testable for all input and output signals stuck-at logic 0 or 1 (sa0 or sa1.) However, a local test-pattern of A for a sa0 fault on its output has both inputs at logic 1. When we apply this pattern to the composite circuit, both inputs of A and the bottom input of B are set to logic 1. The top input of B receives the fault effect 1/0, which means that if the fault is not present, the input is 1, and if it is present, the input is 0. However, the bottom input of 1 for B forces the output of B ($OUT0$) to be logic 1, and blocks observation of the fault effect coming from A. This simple example illustrates that testing is a global problem: Combinations of fully-testable modules in a logic circuit are not necessarily fully-testable, and may not be testable by the same patterns that would test the modules individually. In this case, the output of A sa0 is untestable.

7.4 Definitions

Definitions presented here are common to all ATPG algorithms.

Definition 7.1 *The* fault cone *is the portion of a circuit whose signals are reachable by a forward trace of the circuit topology starting at the fault site.*

Figure 7.12 shows an example circuit, a fault (on the lower fanout of B), the fault cone, the circuit labeling in the five-valued algebra, and the *D-frontier*.

Definition 7.2 *A* forward implication *results when the inputs to a logic gate are sufficiently labeled so that the output can be uniquely determined.*