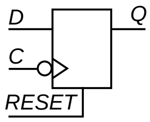

Figure 6.11: Synchronously resettable negative-edge-triggered D flip-flop.

Figure 6.11 shows a synchronously resettable negative-edge-triggered D flip-flop. In order to control the Q line to 1, one must set D to 1, cause a falling clock (C) edge (first a 1 and then a 0), and control the $RESET$ line to 0 to avoid clearing Q. The combinational and sequential difficulties of controlling Q to a 1 are:

$$\begin{aligned} CC1(Q) &= CC1(D) + CC1(C) + CC0(C) + CC0(RESET) \\ SC1(Q) &= SC1(D) + SC1(C) + SC0(C) + SC0(RESET) + 1 \end{aligned} \tag{6.1}$$

$CC1$ measures how many *lines* in the circuit must be set to make Q a 1, whereas $SC1$ measures how many *flip-flops* in the circuit must be clocked to set Q to 1. There are two ways to set Q to a 0. We can either use the $RESET$ line and apply a falling edge to clock C, or clock a 0 into Q through the D line. Thus,

$$\begin{aligned} CC0(Q) &= min \quad [CC1(RESET) + CC1(C) + CC0(C), \\ &\qquad\qquad CC0(D) + CC1(C) + CC0(C)] \\ SC0(Q) &= min \quad [SC1(RESET) + SC1(C) + SC0(C), \\ &\qquad\qquad SC0(D) + SC1(C) + SC0(C)] + 1 \end{aligned} \tag{6.2}$$

The D line can be observed at Q by holding $RESET$ low and generating a falling edge on the clock line C:

$$\begin{aligned} CO(D) &= CO(Q) + CC1(C) + CC0(C) + CC0(RESET) \\ SO(D) &= SO(Q) + SC1(C) + SC0(C) + SC0(RESET) + 1 \end{aligned} \tag{6.3}$$

$RESET$ can be observed by setting Q to a 1 and using $RESET$:

$$\begin{aligned} CO(RESET) &= CO(Q) + CC1(Q) + CC1(RESET) \\ &\quad + CC1(C) + CC0(C) \\ SO(RESET) &= SO(Q) + SC1(Q) + SC1(RESET) + SC1(C) + SC0(C) + 1 \end{aligned} \tag{6.4}$$

There are three ways to indirectly observe the clock line C: (1) set Q to 1 and clock in a 0 from D, (2) set Q to 1 and synchronously apply $RESET$, or (3) set Q to 0 and clock in a 1 from D while holding $RESET$ to 0. Thus,

$$\begin{aligned} CO(C) &= min \quad [CO(Q) + CC1(Q) + CC0(D) + CC1(C) + CC0(C), \\ &\qquad\qquad CO(Q) + CC1(Q) + CC1(RESET) + CC1(C) + CC0(C), \\ &\qquad\qquad CO(Q) + CC0(Q) + CC0(RESET) + CC1(D) + CC1(C) \\ &\qquad\qquad + CC0(C)] \end{aligned} \tag{6.5}$$