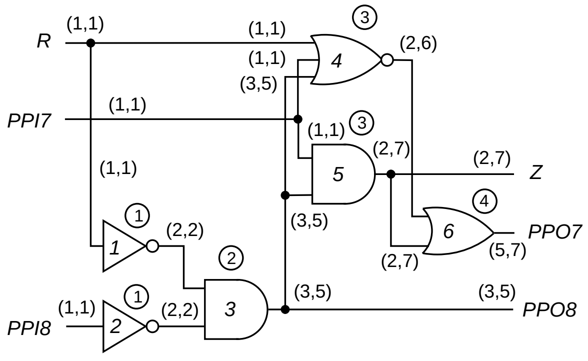

Figure 6.7: Final combinational circuit controllabilities.

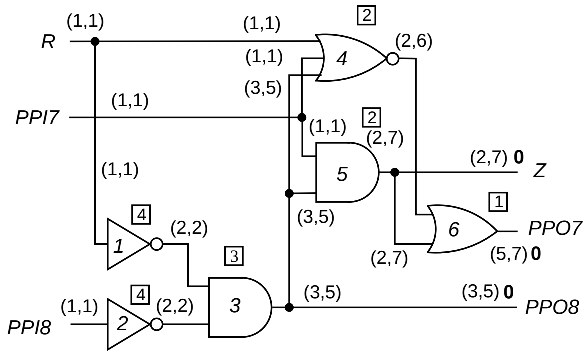

Figure 6.8: Combinational circuit with observabilities through level 1.

We now compute observabilities, which are shown in **boldface** in the figures after the $(CC0, CC1)$ ordered pairs. We process logic gates in level order from POs backwards to PIs. In Figure 6.8, we assign 0 to PO Z and PPOs *PPO7* and *PPO8*. This causes observability 0 to be assigned to gate *6*, as well. We cannot yet assign observabilities to gates *5* and *3*, because they are fanout stems, and not all fanout branch observabilities are known. So, we process OR gate *6* at level 1 in Figure 6.9. For each input, according to Figure 6.3, we have:

$$
\begin{aligned}
CO(4) &= CC0(5) + CO(6) + 1 = 2 + 0 + 1 = 3 \\
CO(5) &= CC0(4) + CO(6) + 1 = 2 + 0 + 1 = 3
\end{aligned}
$$

This is shown in Figure 6.9. Next, we process NOR gate *4* at level 2 in Figure 6.9. According to Figure 6.3, for a three-input NOR gate:

$$
CO(\text{1st input}) = CC0(\text{2nd input}) + CC0(\text{3rd input}) + CO(\text{output}) + 1
$$

Therefore,

$$
\begin{aligned}
CO(R) &= CC0(PPI7) + CC0(3) + CO(4) + 1 = 1 + 3 + 3 + 1 = 8 \\
CO(PPI7) &= CC0(R) + CC0(3) + CO(4) + 1 = 1 + 3 + 3 + 1 = 8 \\
CO(3) &= CC0(R) + CC0(PPI7) + CO(4) + 1 = 1 + 1 + 3 + 1 = 6
\end{aligned}
$$