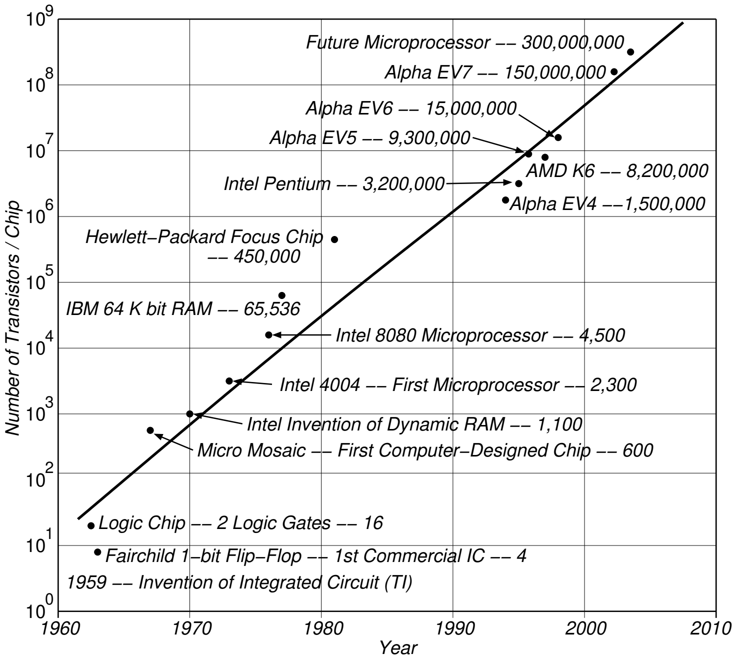

Figure 1.5: VLSI circuit transistor density.

can be placed on the chip is proportional to the chip area, d^2. The number of input/output (I/O) pins, N_p, is proportional to $4d$, since pins are placed on the periphery of the chip. We can thus express an approximate relation between N_p and N_t, as

$$N_p = K\sqrt{N_t} \tag{1.5}$$

where K is a constant. This simple relation was first observed empirically by Rent at IBM and is known as Rent's rule [680]. It has many applications and in Chapter 18, we will use a generalized form (Equation 18.3) to represent the number of terminal signals for a block of logic gates. As we shrink the feature size, for the same chip area, both N_p and N_t increase. But the number of transistors increases faster. Multilayer wiring allows more of the chip area to be utilized by transistors, but does not increase the number of pins, which must be placed at the chip boundary (an exception is the flip-chip technology, not considered here, in which the pins are placed on the chip area [54].) Since any test procedure must now access a larger number of devices (transistors or gates) and interconnects through a proportionately smaller number of pins, the test problem becomes more complex with the higher level of integration. Though it is not a very effective measure, the increase of test complexity is sometimes expressed as the ratio, N_t/N_p. For the data in the second column (1997-2001) of Table 1.1, this ratio for the largest chip is $10^7/900 = 1.1 \times 10^4$. For 2003-2006 and 2009-2012, we get 2.6×10^4 and 6.7×10^4, respectively. This shows the test complexity more than doubling every five or six years.