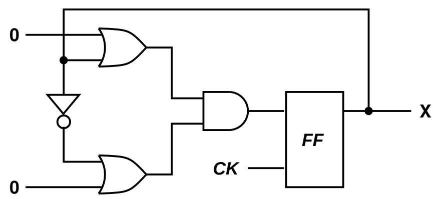

Figure 5.28: Circuit for Problem 5.10.

5.12 Reexamine the cases (a) and (b) of the previous problem for an input pulse of 1 unit width. *Note that the gate filters out a pulse narrower than its own delay – a phenomenon known as spike suppression.*

5.13 Explain what action an event-driven true-value simulator will take when it evaluates a zero-delay gate.

5.14 For implementing an event-driven simulator for unit-delay simulation, what is the minimum number of time slots needed?

5.15 Suppose that the fault coverage increases linearly from 0 to 100% as a large number of vectors is applied. Show that a serial fault simulator will take about half the CPU time with fault dropping than without. Assume that in fault dropping any fault is dropped the first time it is detected.

5.16 Show that when n faults are simulated without fault dropping, a parallel fault simulator on a w-bit word computer will run $(n+1)(w-1)/n$ times faster than a serial fault simulator.

5.17 Assuming a four-bit machine word, demonstrate parallel fault simulation of vector (1,0,1) for the three single stuck-at-1 faults on the second primary input and its two fanouts, respectively, in the circuit of Figure 5.22.

5.18 Derive the output fault list L_c for an exclusive-OR gate, $c = a \oplus b$, in terms of the input fault lists, L_a and L_b.

5.19 Explain why a concurrent fault simulator requires more memory than a deductive fault simulator.

5.20 A VLSI design center is equipped to design digital circuits with embedded memory blocks. The circuits are modeled at the logic level but the simulator must have a four-state (0,1,X,Z) signal representation. Only single stuck-at faults are to be simulated. In order to select a fault simulator, you must answer the following questions:

(a) Which of the simulators among serial, parallel, deductive, and concurrent, can simulate the circuits?

(b) Which is the best choice among these four simulators?