5.5.4 Concurrent Fault Simulation

The concurrent fault simulation algorithm [684, 685] is the most general method of fault simulation. It can handle various types of circuit models, faults, signal states, and timing models. It basically extends the event-driven simulation method to the simulation of faults in the most efficient way.

Let us again consider the fault simulation problem as depicted in Figure 5.14. A concurrent fault simulator models the problem as follows:

1. *Events.* Consider a line (signal) in the fault-free circuit C( ). An event (signal change) on this line is called a *good-event.* Three attributes specify a good-event: line designation (or signal name), type of change (e.g., 0-to-1, or any change among permissible signal states), and the time of change. The same line also exists in faulty circuits, C(f1) through C(fn), and events on it in those circuits, only when they differ from the good-event, are called *fault-events.* A fault event is specified by the same three attributes required for a good-event and an additional designation of the fault (site and type.)

2. *Structure.* The circuit C( ) is modeled in the same way as for the true-value simulation (see Section 5.3.) Any hierarchy is flattened and modules (though referred to as gates in this discussion) can be at any level of abstraction. In general, a module can have internal state variables and multiple outputs. The structure contains the connectivity information (fanouts and fanins) and gate (or module) functions. Each gate is called a *good-gate.* A *fault-list*, usually in the form of a linked-list, is associated with each good-gate. Elements of this list are called *bad-gates.* A bad-gate is not faulty itself but is affected by some fault. At least one of its signals at input or output terminals or internal states differs in value from the corresponding good-gate. The bad-gate derives its name from the fault that causes the signal difference. A bad-gate has the same input-output function as the good-gate since faults are modeled in signals and not in the function. Let us denote faulty circuit gates corresponding to gate g in C( ) as g_i in C(fi), where fi (i = 1, 2, . . . n) are faults being simulated. Suppose, only gates g_6 and g_{18} have any signal differences with g at some time during the simulation, then at that time the fault-list of g will have two bad-gates specified as: (fault f6; terminal values of g_6) and (fault f18; terminal values of g_{18}.) The circuit structure of good-gates with associated fault-lists is a very compact and complete representation of the $n + 1$ circuits shown in Figure 5.14.

3. *Faults.* Faults are assumed to be permanent and affect signal values at terminals or internal states (if any) of modules. The fault information (fault site and type) is stored with the good-gate connected to the fault site. Faults at primary inputs and primary outputs can be modeled by attaching simple buffer gates. Whenever the signal values of a good-gate make a fault active, a bad-gate is inserted in the fault-list of that good-gate.