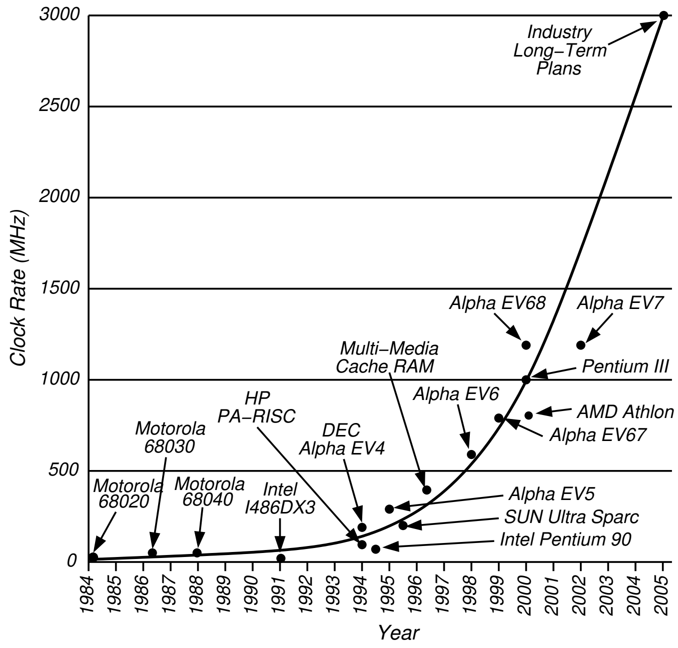

Figure 1.4: Microprocessor clock rates.

We compute the yearly running cost of the ATE by assuming a linear depreciation over five years, and an annual maintenance cost of 2% of the purchase price. The operating cost of the building, facilities, auxiliary equipment (wafer and chip handlers, fixtures, etc.), and personnel is estimated to be $\$0.5M$. Thus:

$$\begin{aligned} Running\ cost &= Depreciation + Maintenance + Operating\ cost \\ &= \$0.854M + \$0.085M + \$0.5M = \$1.439M/year \end{aligned}$$

The tester is used in three eight-hour shifts per day and on all days of the year. Therefore:

$$Testing\ cost = \frac{\$1.439M}{365 \times 24 \times 3,600} = 4.56\ cents/second$$

The test time for a digital ASIC (application specific integrated circuit) is 6 seconds. That gives the test cost as 27.36 cents. Since the bad chips are not sold, their test cost must be recovered from the sale of good chips. If the yield is 65%, then the test component in the sale price of a good chip is 27.36/0.65 $\approx$ 42 cents.

The test time of a chip depends on the types of tests conducted. These may include parametric tests (leakage, contact, voltage levels, etc.) applied at a slow speed, and vector tests (also called "functional tests" in the ATE environment) applied at high speed. The time of parametric tests is proportional