Digital-to-analog converter (DAC)

Figure 54. DAC channel block diagram

Table 55. DAC pins

- DAC Init
  - clock for GPIO pin
  - clock for DAC
  - GPIO pin mode analog
  - enable DAC

DAC = DHR12R1 = data

Ex: DAC = DHR12R1 = data

Table 55. DAC pins

+ Single Channel Data Reg.
  (Also "double" value registers)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>DAC_DHR8RX[7:0] (8-bit sample)</td>
</tr>
<tr>
<td>12</td>
<td>DAC_DHR12RX[11:0] (12-bit sample)</td>
</tr>
<tr>
<td>8</td>
<td>DAC_DHR12LX[11:0]</td>
</tr>
</tbody>
</table>

Double Convert:
31 8 23 15 8 7 8

Vref x DOR / 4095 (12-bit)
DAC_CSR: [31:16, 15:0]

- DMAUDRIE: DMA "under-run" error infr. enable
  (new request before last data used)
- DMAENx: DMA enable
- MAMPx: generate triangle/LFSR noise waveforms
- WAVEy: waveforms
- TSELx [2:0]: trigger select
- TENVx: trigger enable
  (0: write to DHRx in one cycle)
- TRG: trigger D/A conversion
  (DHRx -> DORx Xfer)
- SWTR10: setting this bit start convert.
- BOFFx: output buffer disable
- ENx: enable DAC x

DAC_CSR: [31:16, 15:0]

DAC_DHR12R1: 12-bit data holding reg/right aligned

DAR2R: bit 29 = DMAUDR2
bit 13 = DMAUDR1

Note: Dual-DAC conversion also supported.