History of Programmable Logic

• Programmable Logic Arrays ~ 1970
  – Incorporated in VLSI devices
  – Can implement any set of SOP logic equations
    • Outputs can share common product terms

• Programmable Logic Devices ~ 1980
  – MMI Programmable Array Logic (PAL)
    • 16L8 – combinational logic only
      – 8 outputs with 7 programmable PTs of 16 input variables
    • 16R8 – sequential logic only
      – 8 registered outputs with 8 programmable PTs of 16 input variables
  – Lattice 16V8
    • 8 outputs with 8 programmable PTs of 16 input variables
      – Each output programmable to use or bypass flip-flop
  – Complex PLDs – arrays of PLDs with routing network

• Field Programmable Gate Arrays ~ 1985
  – Xilinx Logic Cell Array (LCA)

• CPLD & FPGA architectures became similar ~ 2000
PLD Basic Structure

- Programmable product terms (AND plane)
  - AND gates can connect to any input/FF bit or bit-bar
- Fixed OR plane determine maximum # PTs
- Programmable macrocell
  - XOR gate selects SOP or POS for fewer PTs
  - FF for sequential logic or bypass for combinational logic
  - Feedback current state into array for FSM design
Field Programmable Gate Arrays

- Configuration Memory
- Programmable Logic Blocks (PLBs)
- Programmable Input/Output Cells
- Programmable Interconnect

Typical Complexity = 5M – 1B transistors
Basic FPGA Operation

Write Configuration Memory

• Defines system function
  – Input/Output Cells
  – Logic in PLBs
  – Connections between PLBs & I/O cells

Changing configuration memory data ⇒ changes system function

• Can change at anytime
  – Even while system function is in operation
  – Run-time reconfiguration (RTR)
Basic PLB Architecture

• Look-up Table (LUT) implements truth table

• Memory elements:
  – Flip-flop/latch
  – Some FPGAs - LUTs can also implement small RAMs

• Carry & control logic implements fast adders/subtractors
Combinational Logic Functions

- Gates are combined to create complex circuits
- Multiplexer example
  - If $S = 0$, $Z = A$
  - If $S = 1$, $Z = B$
  - Very common digital circuit
  - Heavily used in FPGAs
    - $S$ input controlled by configuration memory bit
    - We’ll see it again
Look-up Tables

• Recall multiplexer example
• Configuration memory holds outputs for truth table
• Internal signals connect to control signals of multiplexers to select value of truth table for any given input value
Look-up Table Based RAMs

- Normal LUT mode performs read operations
- Address decoder with write enable generates clock signals to latches for write operations
- Small RAMs but can be combined for larger RAMs
A Simple PLB

- **Two 3-input LUTs**
  - Can implement any 4-input combinational logic function

- **1 flip-flop**
  - Programmable:
    - Active levels
    - Clock edge
    - Set/reset

- **22 configuration memory bits**
  - 8 per LUT
    - C0-7
    - S0-7
  - 6 controls
    - CB0-7
Interconnect Network

• Wire segments of varying length
  – $xN = N$ PLBs in length
    • 1, 2, 4, 6, and 8 are most common
  – $xH = \text{half the array in length}$
  – $xL = \text{length of full array}$

• Programmable Interconnect Points (PIPs)
  • Also known as Configurable Interconnect Points (CIPs)
  – Transmission gate connects to 2 wire segments
  – Controlled by configuration memory bit
    • 0 = wires disconnected
    • 1 = wires connected
PIPs

• Break-point PIP
  – Connect or isolate 2 wire segments

• Cross-point PIP
  – Turn corners

• Compound cross-point PIP
  – Collection of 6 break-point PIPs
    • Can route to two isolated signal nets

• Multiplexer PIP
  – Directional and buffered
  – Select 1-of-$N$ inputs for output
    • Decoded MUX PIP – $N$ config bits select from $2^N$ inputs
    • Non-decoded MUX PIP – 1 config bit per input
Spartan 3 Routing Resources

- PLB consists of 4 slices
- 2 LUTs & 2 FFs/slice
- switch matrix
  - over 2,400 PIPs
  - mostly MUX PIPs
- x6 wire segments
- x2 wire segments
- xH & xL wire segments
- over 450 total wire segments in PLB
Input/Output Cells

• Bi-directional buffers
  – Programmable for input or output
  – Tri-state control for bi-directional operation
  – Flip-flops/latches for improved timing
    • Set-up and hold times
    • Clock-to-output delay
  – Pull-up/down resistors

• Routing resources
  – Connections to core of array

• Programmable I/O voltage & current levels
FPGAs

• Recent trend - incorporate specialized cores
  – RAMs – single-port, dual-port, FIFOs
    • 128 bits to 36K bits per RAM
    • 4 to 575 per FPGA
  – DSPs – 18x18-bit multiplier, 48-bit accumulator, etc.
    • up to 512 per FPGA
  – Microprocessors and/or microcontrollers
    • up to 2 per FPGA
      – Hard core processor
    • Support soft core processors
      – Synthesized from HDL into programmable resources
Spartan 3 (XC3S200)

- 24 rows x 20 columns = 480 PLBs
  - 4 slices/PLB
  - 2 LUTs&FFs/slice
- 12 18K-bit dual port RAMs
- 12 18x18-bit multipliers
# Ranges of Resources

<table>
<thead>
<tr>
<th>FPGA Resource</th>
<th>Small FPGA</th>
<th>Large FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLBs per FPGA</td>
<td>256</td>
<td>25,920</td>
</tr>
<tr>
<td>LUTs and flip-flops per PLB</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>Routing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wire segments per PLB</td>
<td>45</td>
<td>406</td>
</tr>
<tr>
<td>PIPs per PLB</td>
<td>139</td>
<td>3,462</td>
</tr>
<tr>
<td>Specialized Cores</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits per memory core</td>
<td>128</td>
<td>36,864</td>
</tr>
<tr>
<td>Memory cores per FPGA</td>
<td>16</td>
<td>576</td>
</tr>
<tr>
<td>DSP cores</td>
<td>0</td>
<td>512</td>
</tr>
<tr>
<td>Other</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input/output cells</td>
<td>62</td>
<td>1,200</td>
</tr>
<tr>
<td>Configuration memory memory bits</td>
<td>42,104</td>
<td>79,704,832</td>
</tr>
</tbody>
</table>