Research Seminar Series

Monday, August 21st, 2006  3-3:50pm, 112 Thatch Hall

Testing Process Interactions to Support Hierarchical Hardware Verification

All hardware designs depend on structural hierarchy to manage complexity. Each system is constructed as a structural interconnection of a set of components, and it is the interaction of the components which defines the behavior of the system. Hardware verification typically requires over 70% of the total design effort so it is essential that the existing structural hierarchy by leveraged for verification as well. The hierarchical verification problem is divided into unit testing, the verification of individual components, and interaction testing, the verification of the interactions between components. We investigate the problem of interaction testing by defining a coverage metric to estimate the degree to which component interactions have been verified by a given test set. Coverage metrics which evaluate processes separately are unlikely to model the range of design errors which manifest when components are integrated to build a system. A metric which models component interactions is essential to enable verification techniques to scale with growing design complexity. We describe the effectiveness of our metric and results demonstrate that coverage using our metric is computationally tractable.

The large number of potential interactions between processes must be managed in order to make the testing process tractable. Fortunately, many potential interactions are actually infeasible and should be ignored during the testing process. Data dependency between processes indicates the potential for a feasible interaction but absolute feasibility can only be determined by evaluating control-flow paths through interacting processes. We propose a method to identify feasible transactions for testing through static analysis combined with the use of a Constraint Satisfaction Programming (CSP) solving engine.

Ian G. Harris, PhD
University of California Irvine.