Gate-Controlled Punch Through Transistor

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Abstract—Operation of the gate-controlled punch through transistor is demonstrated in this paper. The characteristics of the device are simulated using SILVACO atlas device simulator. This device shows high voltage, high operation frequency, and low noise properties. This punch through device can be used in high power control circuit, and also can be used for fast analog circuits for multiplication, squaring and root calculation.

I. INTRODUCTION

THE static induction devices were invented by Nishizawa. [1] The number of devices in this family continues to grow with time. The static induction devices have many advantages over the traditional devices, and static induction devices exhibit high voltage and high frequency operation, low distortion and low noise performances compared to that of BJT and FET. [2-4]

Punch through transistor belongs to the static induction device family. For punch through transistors, the carriers transit time is very small; therefore, operation frequency can be very high. Also punch-through transistors are very resistant to thermal breakdown because of negative temperature feedback at high current levels. [5]

Several kinds of punch through transistor structure were published, such as punch through transistor with MOS controlled gate, lateral punch through transistor. [6-7] In this paper, the new structure of gate controlled punch-through transistor is proposed and simulated using SILVACO atlas device simulator. The punch through transistors can be used widely in high voltage power electronics. The drain current can be controlled by both gate and drain voltage. Also by changing the geometry spacing of the terminal, different voltage multiplication factor transistors can be fabricated. This kind of punch through transistor is much simpler to fabricate using the current technology than other static induction devices. This paper starts with the introduction to the operation principle of the punch through transistor. Then one gate-controlled punch through transistor structure is proposed and the characteristics simulation of the device is performed using SILVAVO atlas device simulator.

II. OPERATION PRINCIPLE OF PUNCH THROUGH TRANSISTOR

The cross section of static induction transistor is shown in Fig. 1. An induced electrostatic potential barrier controls the current in static induction transistor. The carriers injected from the source pass the potential barrier and move toward the drain with limited velocity. These carriers create the space charge between the potential barrier and drain. The derivations of formulas are done for n-channel device, but the obtained results with a little modification can be applied for p-channel devices.

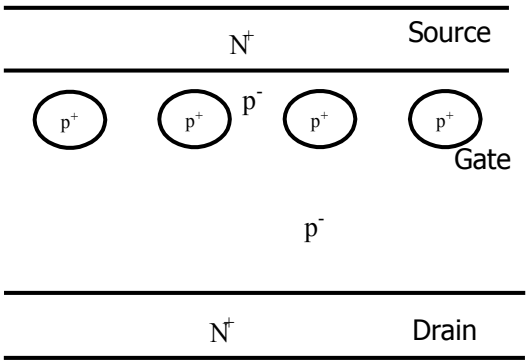


Fig. 1 Cross section of the static induction transistor

For a small electrical field existing in the vicinity of the potential barrier, the drift and diffusion current can be approximated by [3]

$$J_n = -qn(x)\mu_n \frac{d\varphi(x)}{dx} + qD_n \frac{dn(x)}{dx} \tag{1}$$

Where $D_n = \mu_n V_T$ and $V_T = \frac{kT}{q}$. By multiplying both sides of the equation by $\exp(-\varphi(x)/V_T)$ and rearranging

$$J_n \exp(-\frac{\varphi(x)}{V_T}) = qD_n \frac{d}{dx}\left[n(x)\exp(-\frac{\varphi(x)}{V_T}) \right] \tag{2}$$

By integrating from $x1$ to $x2$, one can obtain

$$J_n = qD_n \frac{n(x_2)\exp(-\varphi(x_2)/V_T) - n(x_1)\exp(-\varphi(x_1)/V_T)}{\int_{x_1}^{x_2} \exp(-\varphi(x)/V_T)dx} \tag{3}$$

With the following boundary conditions

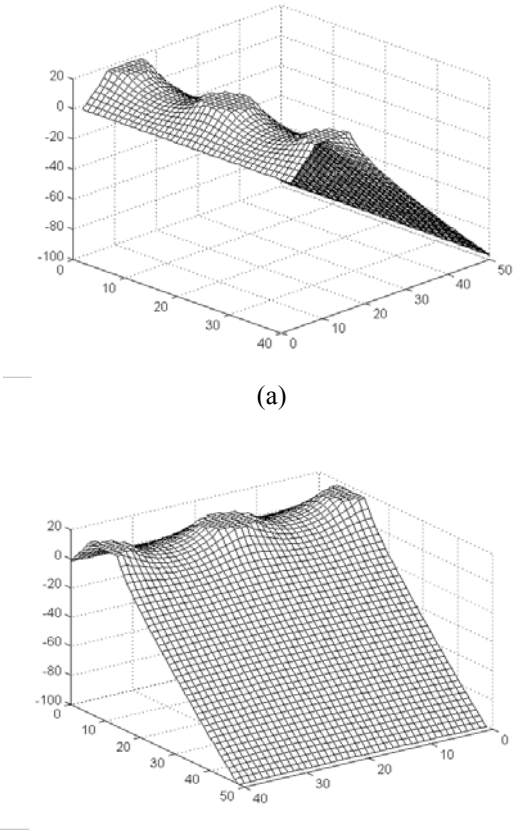
$\varphi(x_1) = 0;$ $\quad n(x_1) = N_S$

$$\varphi(x_2) = V_D; \qquad n(x_2) = N_D \tag{4}$$

We can get the following result for the current density.

$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right) dx} \tag{5}$$

Note that the preceding equations also can be used to find current in any devices controlled by a potential barrier, such as a bipolar transistor or a MOS transistor operation in sub-threshold mode, or in Schottky diode.



(a)

(b)

Fig.2 Potential distribution of the static induction transistor: (a) view from the source side; (b) view from the drain side.

Samples of the potential distribution are shown in Fig. 2. The vicinity of the barrier was approximated by Plotka[8,9] by using parabolic formulas along and cross the channel. Fig. 3 shows the potential distribution in the vicinity of the barrier approximated by parabolic shapes.

$$\varphi(x) = \Phi\left(1 - \left(2\frac{x}{L} - 1\right)^2\right) \tag{6}$$

$$\varphi(y) = \Phi\left(1 - \left(2\frac{y}{W} - 1\right)^2\right) \tag{7}$$

Integrating equation (5) first along the channel and then across the channel yields a very simple formula for drain currents in n-channel transistors

$$I_D = qD_p N_S Z \frac{W}{L} \exp\left(\frac{\Phi}{V_T}\right) \tag{8}$$

Where Φ is the potential barrier height in reference to the source potential, N_S is the electron concentration at the source, the W/L ratio describes the shape of the potential saddle in the vicinity of the barrier, and Z is the length of the source strip.

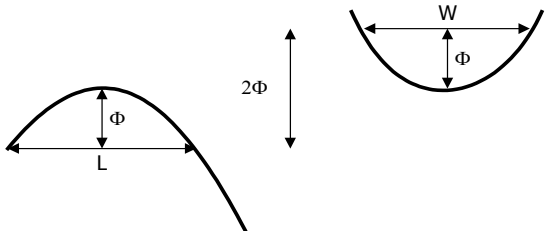


Fig.3 Potential distribution in the vicinity of the barrier approximated by parabolic shapes.

As the barrier height Φ can be a linear function of gate and drain voltages,

$$I_D = qD_p N_s Z \frac{W}{L} \exp\left(\frac{a(V_{GS} + bV_{DS} + \Phi_0)}{V_T}\right) \tag{9}$$

Equation (9) describes the drain current characteristics for a small current range. For large current, it is controlled by the space charge of moving carriers. In the one-dimensional (1D) case the potential distribution is described by the Poisson equation: [5]

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} \tag{10}$$

Where the charge density $\rho(x)$ is:

$$\rho(x) = \frac{Q}{\Delta x} = \frac{I_D \tau}{\Delta x} = \frac{J}{v(x)} \tag{11}$$

Carrier velocity $v(x)$ for a small and moderate electrical field is

$$v(x) = \mu E(x) \tag{12}$$

Solving (10) for small and moderate electrical fields (boundary conditions: $E = 0$, $V = 0$ at $x = 0$) yields:

$$I_D = \frac{9}{8} V_{DS}^2 \mu \varepsilon_{Si} \varepsilon_0 \frac{A}{L^3} \tag{13}$$

$$\tau = \frac{4}{3} \frac{L^2}{V_D \mu} \tag{14}$$

And for a large electrical field, $v(x) = const.$, the equation (10) results in:

$$I_D = 2V_{DS} v_{sat} \mu \varepsilon_{Si} \varepsilon_0 \frac{A}{L^2} \tag{15}$$

$$\tau = \frac{L}{v_{sat}} \tag{16}$$

Where L is the channel length and $v_{sat} = 10^7 cm/s$ is the carrier saturation velocity.

For the punch through transistor, the characteristics follow the space charge conduction law for a wide range. The current voltage relationship is described by an exponential relationship equation (9) for small currents, a quadratic relationship equation (13), and finally, for large voltages by an almost linear relationship equation (15).

III. PROPOSED DEVICE STRUCTURE AND SIMULATION

Several structures of gate-controlled punch through transistor are simulated using SILVACO atlas device simulator in this paper. Figure 4 shows one of the structures of N+PN+ gate-controlled punch through transistor. In this structure, the substrate is p-type. The drain and source are N type doping with concentration of 1E20cm^{-3}. There are two connected gates in this structure. The spacing between the gates and the drain, the spacing between the two gates, and the contact potential of the gates control the drain current of the device.

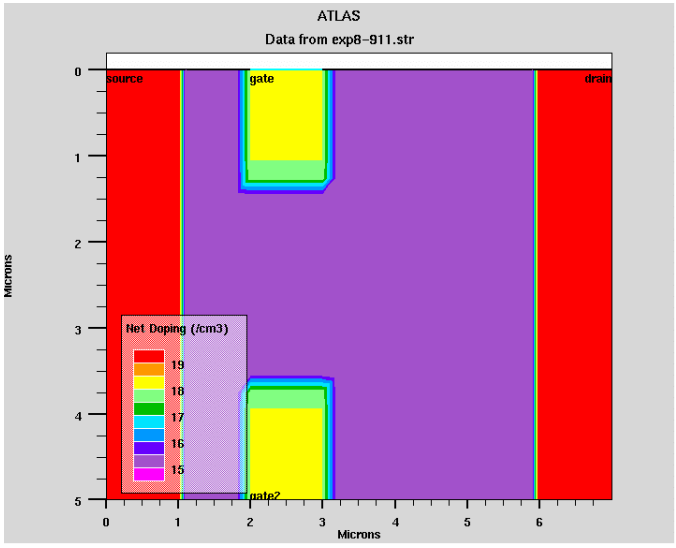


Fig. 4 structure of the gate-controlled punch through transistor

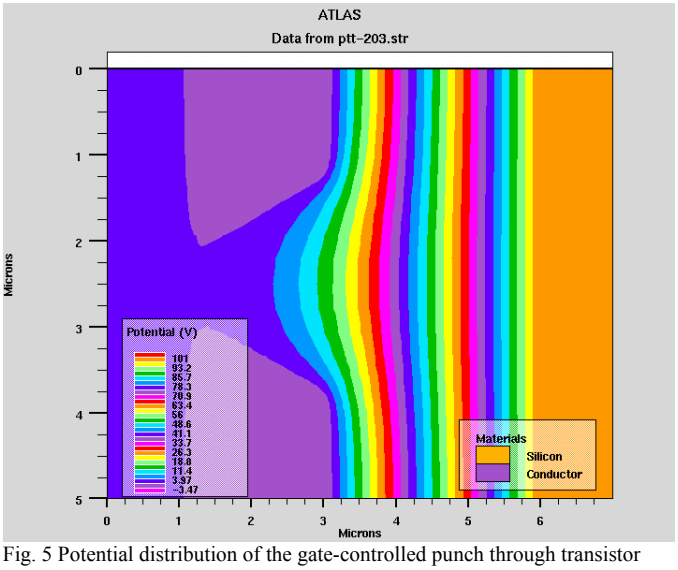


Fig. 5 Potential distribution of the gate-controlled punch through transistor

Fig.5 shows the potential distribution of the device. It is observed that the gate potential barrier controls the current from the drain to the source. Fig. 6 and Fig.7 show characteristics of the drain current in linear scale and log scale separately. From the Fig. 6 and Fig. 7, it is observed that when the current is small, the current increases with the voltage increasing in exponential curve. When the drain bias is close to the punch-through voltage, the relationship between the drain current and voltage changes to quadratic. With the voltage increasing further it changes to linear relationship. Meanwhile, Fig. 6 and Fig. 7 show that with the gate voltage increasing, the punch through voltage also increases.

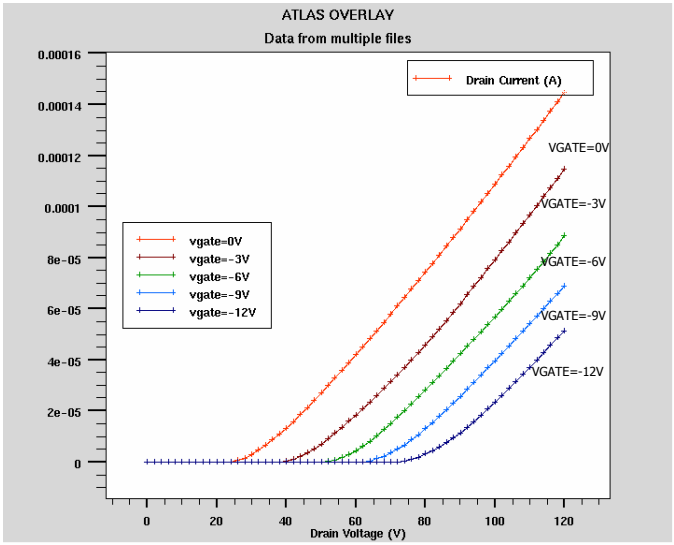


Fig. 6 drain current characteristics of the device with different gate control voltage in linear scale

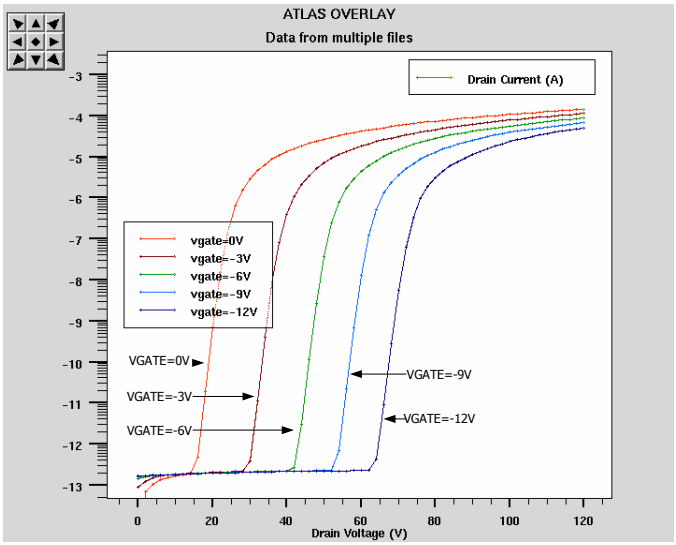


Fig. 7 drain current characteristics of the device with different gate control voltage in log scale

Fig.8 shows the drain current characteristics of the device with different gate and drain spacing. It is observed that the spacing has very strong control to the punch through transistor characteristics. When the spacing between the gates and the drain increases, the depletion region spacing increases, and the punch through voltage increases accordingly. Fig 9 shows the drain current characteristics at different gates spacing. The spacing between the gates controls the shape of the potential barrier. With the gates spacing going down, the average potential barrier goes up, the punch though voltage goes up accordingly.

The voltage amplification factor *m* depends on the transistor geometry, and varies very slightly with transistor bias point.

Therefore, the drain current of the device for the various gate biasing can be described as the following equation [5]

$$I_D = \frac{9}{8}\mu\varepsilon_{Si}\varepsilon_0 \frac{A}{L^3}\left(V_{DS} - mV_G - V_o\right)^2 \qquad (17)$$

where V_0 is the voltage required to achieve punch-through. Equation (17) can describe the gate-controlled punch-through transistor in a very wide current range.

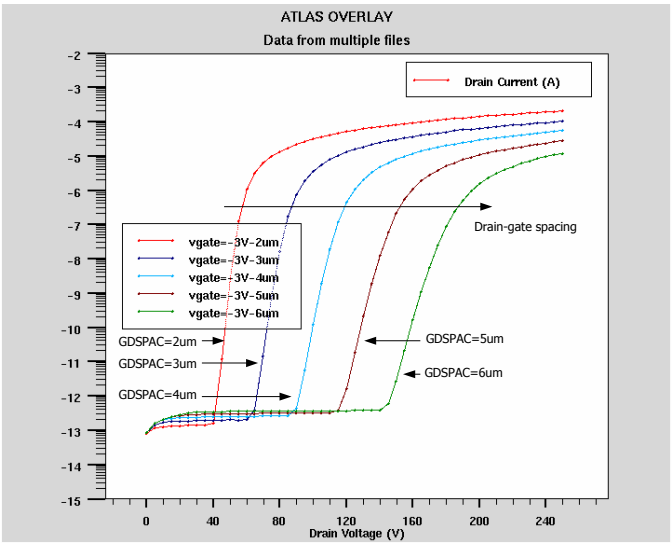


Fig. 8 drain current characteristics with different spacing between the gates and the drain in log scale

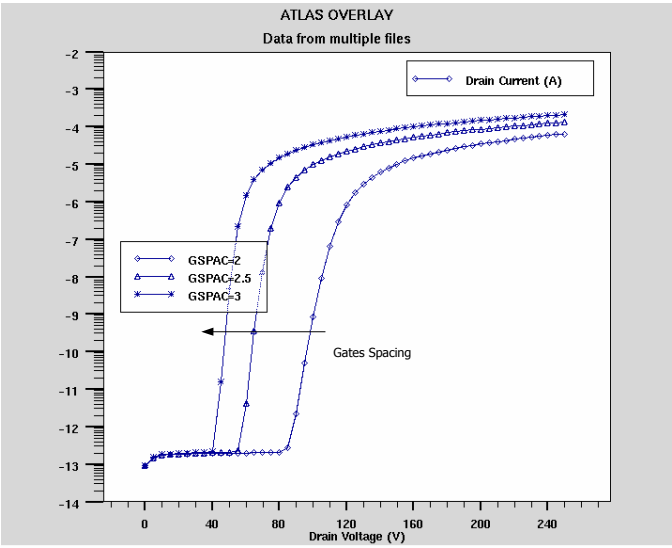


Fig. 9 drain current characteristics with different spacing between the two gates in log scale

Fig. 10 shows the drain current characteristics at different temperature. This shows that the punch through transistor has negative feedback temperature properties. It is observed that, when the device working at high current level, the temperature increasing, drain current then decreases, which causes the device to consume less power. This is a very promising characteristic for the power devices.

With the dimension scales down, all the carriers are transporting in saturation velocity. So this device can work in a very high frequency range. Also the drain, source and gate of the device are surrounded by depletion region, this leads the parasitic junction capacitance very small. This is very promising property for fast operation.

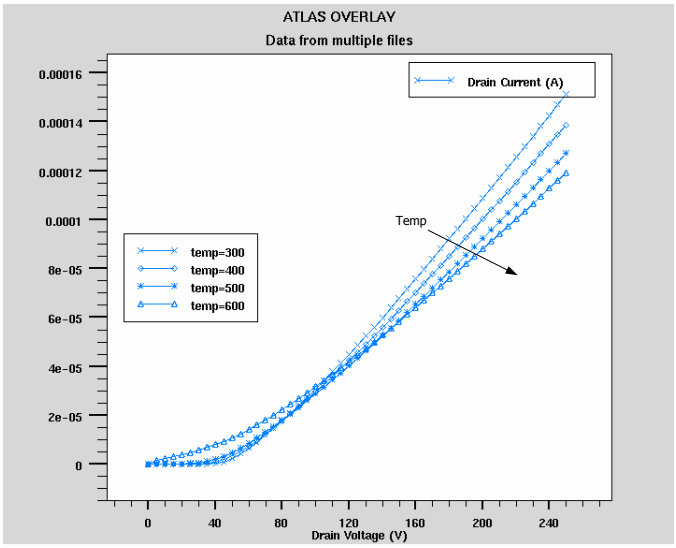


Fig. 10 drain current characteristics at different temperature

IV. Conclusion

The characteristics of this device follow the space charge conduction square law over a very wide current range. This punch-through device can be used in high power control circuit, and also can be used for fast analog circuits for multiplication, squaring and root calculation.

V. Acknowledgement

The authors gratefully acknowledge Idaho NASA ESPCoR for its full support.

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