9

Static Induction Devices

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Summary

Several devices from the static induction family including static induction transistors (SIT), static induction diodes (SID), static induction thyristors, lateral punch-through transistors (LPTT), static induction transistor logic (SITL), static induction MOS transistors (SIMOS), and space charge limiting load (SCLL) are described. The theory of operation of static induction devices is given for both a current controlled by a potential barrier and a current controlled by space charge. The new concept of a punch-through emitter (PTE), which operates with majority carrier transport, is presented.

9.1 Introduction

Static induction devices were invented by Nishizawa [28]. The idea was so innovative that the establishment in the solid-state electronics community at the time had difficulty understanding and accepting this discovery. Japan was the only country where static induction family devices were successfully fabricated [14]. The number of devices in this family continues to grow with time. Static induction transistors can operate with a power of 100 kW at 100 kHz or 10 W at 10 GHz. Static induction transistor logic had switching energy 100 × smaller than its I^2L competitor [8, 9]. The static induction thyristor has many advantages over the traditional SCR, and the static induction diode exhibits high switching speed, large reverse voltage, and low forward voltage drops.

9.2 Theory of Static Induction Devices

The cross section of the static induction transistor is shown in Fig. 9.1, while its characteristics are shown in Fig. 9.2. An induced electrostatically potential barrier controls the current in static induction devices. The derivations of formulas will be done for an n-channel device, but the obtained results with a little modification also can be applied to p-channel devices. For a small electrical field existing in the vicinity of the potential barrier, the drift and diffusion current can be approximated by

$$J_n = -qn(x)\mu_n \frac{d\varphi(x)}{dx} + qD_n \frac{dn(x)}{dx} \tag{9.1}$$

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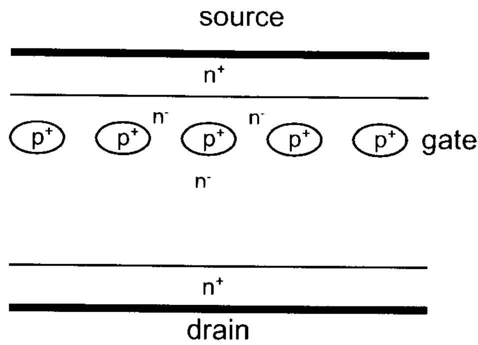


FIGURE 9.1 Cross section of the static induction transistor.

where $D_n = \mu_n V_T$ and $V_T = kT/q$. By multiplying both sides of the equation by $\exp(-\varphi(x)/V_T)$ and rearranging

$$J_n \exp\left(-\frac{\varphi(x)}{V_T}\right) = qD_n \frac{d}{dx}\left[n(x)\exp\left(-\frac{\varphi(x)}{V_T}\right)\right] \quad (9.2)$$

By integrating from x_1 to x_2, one can obtain

$$J_n = qD_n \frac{n(x_2)\exp(-\varphi(x_2)/V_T) - n(x_1)\exp(-\varphi(x_1)/V_T)}{\int_{x_1}^{x_2} \exp(-\varphi(x)/V_T)dx} \quad (9.3)$$

With the following boundary conditions

$$\begin{aligned} \varphi(x_1) &= 0; & n(x_1) &= N_S; \\ \varphi(x_2) &= V_D; & n(x_2) &= N_D; \end{aligned} \quad (9.4)$$

Equation (9.3) reduces to

$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2} \exp(-\varphi(x)/V_T)dx} \quad (9.5)$$

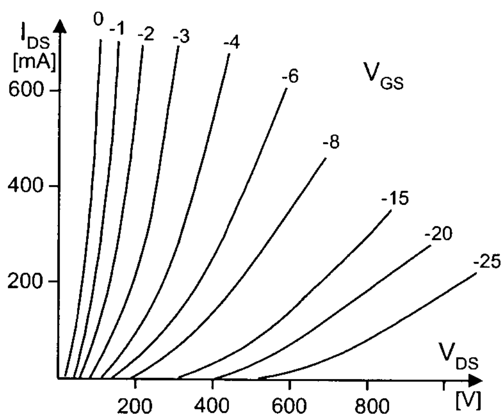


FIGURE 9.2 Characteristics of the early SIT design [7].

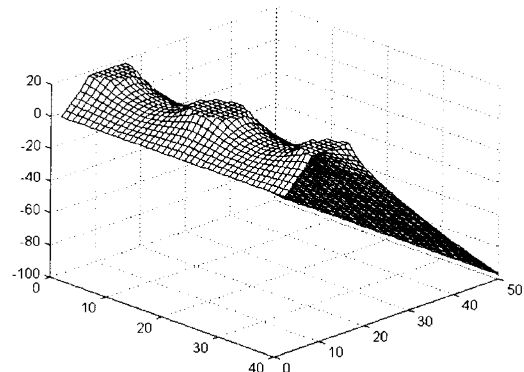
Note that the preceding equations derived for SIT also can be used to find current in any devices controlled by a potential barrier, such as a bipolar transistor or a MOS transistor operating in subthreshold mode, or in a Schottky diode.

9.3 Characteristics of Static Induction Transistor

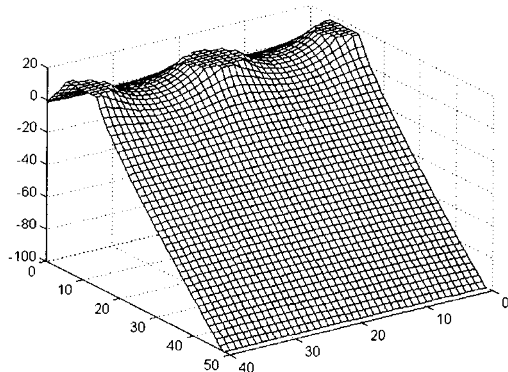
Samples of the potential distribution in SI devices are shown in Fig. 9.3 [1, 20]. The vicinity of the potential barrier was approximated by Plotka [11, 12] by using parabolic formulas (Fig. 9.4) along and across the channel.

$$\varphi(x) = \Phi\left[1 - \left(2\frac{x}{L} - 1\right)^2\right] \quad (9.6)$$

$$\varphi(y) = \Phi\left[1 - \left(2\frac{y}{W} - 1\right)^2\right] \quad (9.7)$$



(a)



(b)

FIGURE 9.3 Potential distribution in SIT: (a) view from the source side; and (b) view from the drain side.

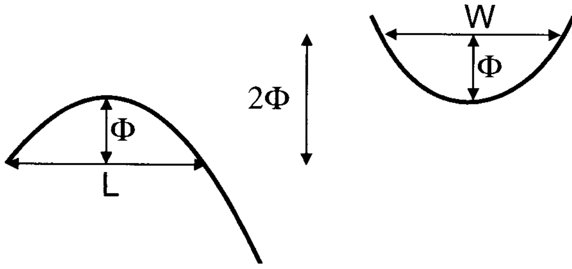


FIGURE 9.4 Potential distribution in the vicinity of the barrier approximated by parabolic shapes.

Integrating Eq. (9.5) first along the channel and then across the channel yields a very simple formula for drain currents in n-channel SIT transistors

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(\frac{\Phi}{V_T}\right) \tag{9.8}$$

where Φ is the potential barrier height in reference to the source potential, N_S is the electron concentration at the source, the W/L ratio describes the shape of the potential saddle in the vicinity of the barrier, and Z is the length of the source strip.

As barrier height Φ can be a linear function of gate and drain voltages,

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(\frac{a(V_{GS} + bV_{DS} + \Phi_0)}{V_T}\right) \tag{9.9}$$

Equation (9.9) describes the characteristics of a static induction transistor for small current range. For large current levels the device current is controlled by the space charge of moving carriers. In the one-dimensional (1D) case the potential distribution is described by the Poisson equation:

$$\frac{d^2\varphi}{dx_2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} = \frac{I_{DS}}{Av(x)} \tag{9.10}$$

Where A is the effective device cross section and $v(x)$ is carrier velocity. For a small electrical field $v(x) = \mu E(x)$ and the solution of Eq. (9.10) is

$$I_{DS} = \frac{9}{8}V_{DS}^2\mu\varepsilon_{Si}\varepsilon_0\frac{A}{L^3} \tag{9.11}$$

and for a large electrical field $v(x) = \text{const}$ and Eq. (9.10) results in:

$$I_{DS} = 2V_{DS}v_{sat}\varepsilon_{Si}\varepsilon_0\frac{A}{L^2} \tag{9.12}$$

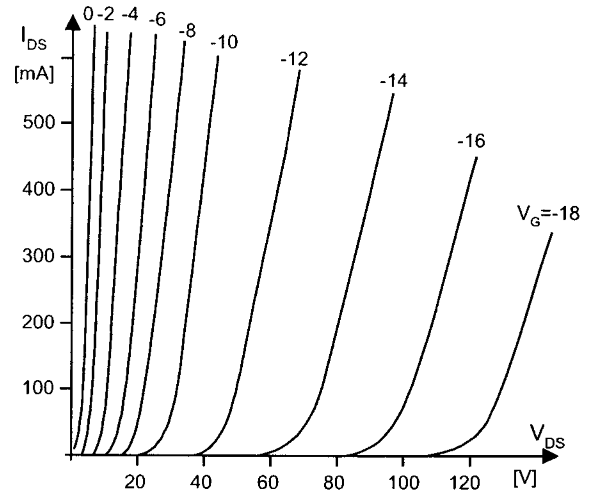


FIGURE 9.5 Characteristics of the static induction transistor drawn in linear scale.

where L is the channel length and $v_{sat} \approx 10^{11}$ μm/s is the carrier saturation velocity. In practical devices the current-voltage relationship is described by an exponential relationship Eq. (9.9) for small currents, a quadratic relationship eq. (9.11), and, finally, for large voltages by an almost linear relationship Eq. (9.12). The SIT characteristics drawn in linear and logarithmic scales are shown in Fig. 9.5 and Fig. 9.6, respectively.

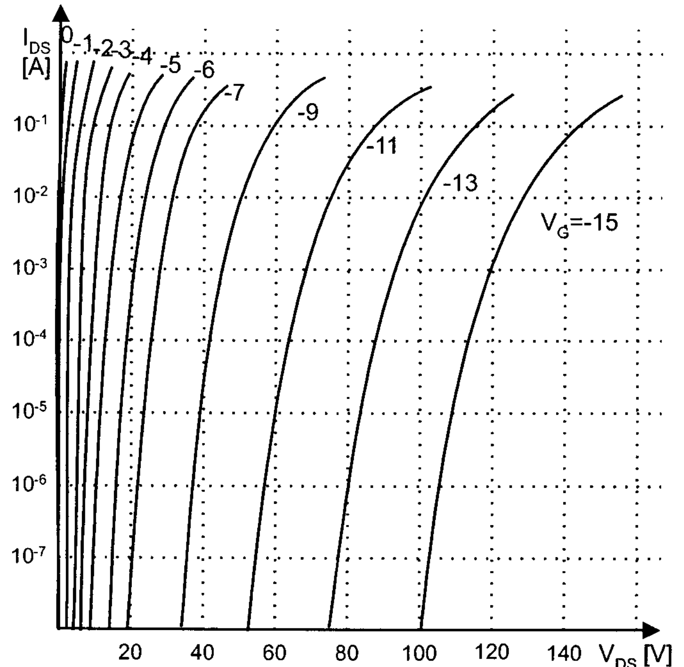


FIGURE 9.6 Characteristics of the static induction transistor drawn in logarithmic scale.

9.4 Bipolar Mode Operation of SI devices (BSIT)

The bipolar mode of operation of SIT was first reported in 1976 by Nishizawa and Wilamowski [8, 9]. Several complex theories for the bipolar mode of operation were developed [2, 5, 6, 10, 23, 24], but actually the simple Eq. (9.5) works well not only for the typical mode of the SIT operation, but also for the bipolar mode of the SIT operation. Furthermore, the same formula works very well for classical bipolar transistors. Typical characteristics of the SI transistor operating in both normal and bipolar modes are shown in Figs. 9.7 and Fig. 9.8.

A potential barrier controls the current in the SIT and it is given by

$$J_n = \frac{qD_nN_S}{\int_{x_1}^{x_2} \exp(-\varphi(x)/V_T)dx} \tag{9.13}$$

where $\varphi(x)$ is the profile of the potential barrier along the channel.

For example, in the case of *npn* bipolar transistors the potential distribution across the base in reference to emitter potential at the reference impurity level $N_E = N_S$ is described by:

$$\varphi(x) = V_T \ln\left(\frac{N_B(x)N_S}{n_i^2}\right) \exp\left(-\frac{V_{BE}}{V_T}\right) \tag{9.14}$$

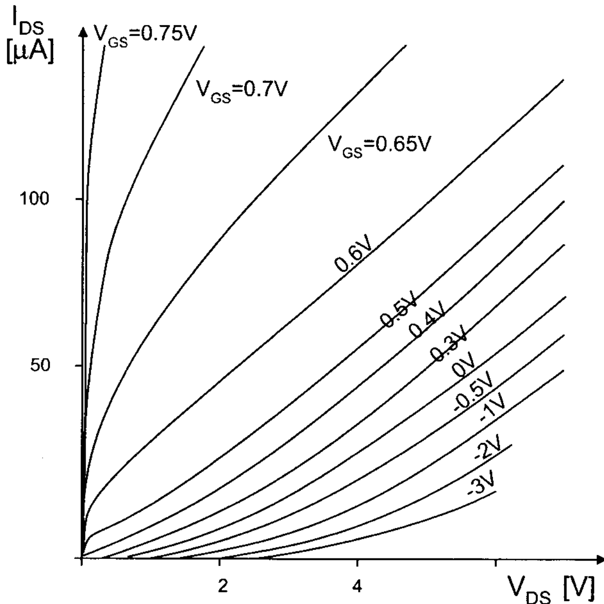


FIGURE 9.7 Small-sized SIT transistor characteristic, operating in both normal and bipolar modes, $I_D = f(V_{DS})$ with V_{GS} as parameter.

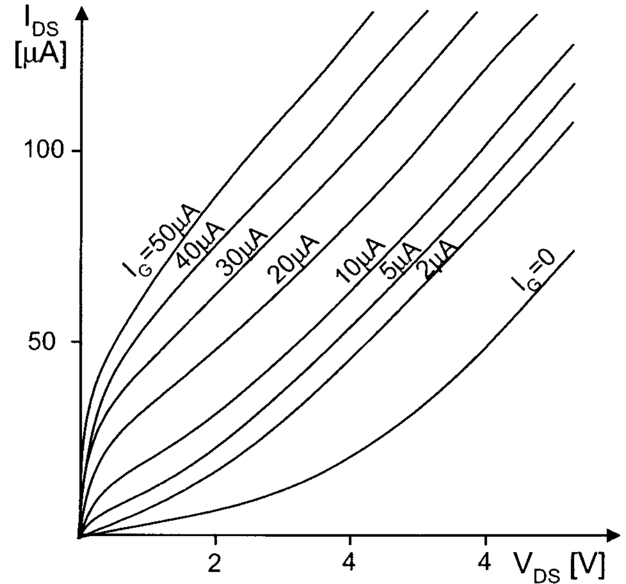


FIGURE 9.8 Small-sized SIT transistor characteristic, operating in both normal and bipolar modes, $I_D = f(V_{DS})$ with I_G as a parameter.

After inserting Eq. (9.14) into (9.13) one can obtain the well-known equation for electron current injected into the base

$$J_n = \frac{qD_nn_i^2}{\int_{x_1}^{x_2} N_B(x)dx} \exp\left(\frac{V_{BE}}{V_T}\right) \tag{9.15}$$

If Eq. (9.13) is valid for SIT and BJT then one may assume that it is also valid for the bipolar mode of operation of the SIT transistor. This is a well-known equation for the collector current in the bipolar transistor, but this time it was derived using the concept of current flow through a potential barrier.

9.5 Emitters for Static Induction Devices

One of the disadvantages of the SIT is the relatively flat shape of the potential barrier (Fig. 9.9a). This leads to slow, diffusion-based transport of carriers in the vicinity of the potential barrier. The carrier transit time can be estimated using the formula:

$$t_{\text{transit}} = \frac{l_{\text{eff}}^2}{D} \tag{9.16}$$

where l_{eff} is the effective length of the channel and $D = \mu V_T$ is the diffusion constant. In the case of a traditional SIT transistor this channel length is $\approx 2\,\mu\text{m}$, while in the case of SIT transistors with sharper barriers (Fig. 9.9b) the channel length is reduced to about $\approx 0.2\,\mu\text{m}$. The corresponding transient times are 2 ns and 20 ps respectively.

The potential distributions shown in Fig. 9.3 are valid for SIT with an emitter made of a traditional *p-n* junction. A

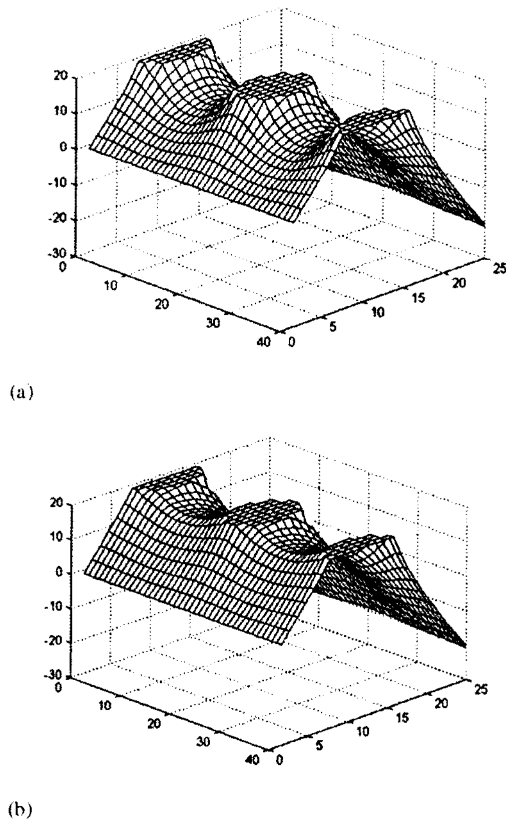


FIGURE 9.9 Potential distributions in SIT: (a) traditional; and (b) with sharp potential barrier.

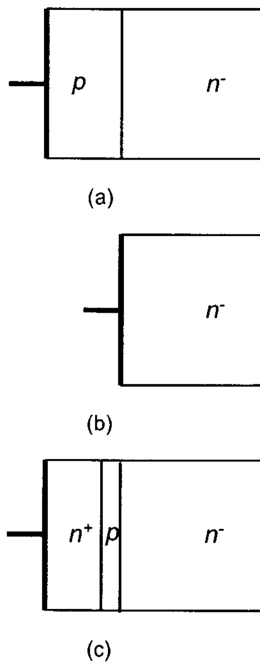


FIGURE 9.10 Various structures of emitters: (a) *p-n* junction including heterostructure with SiGe materials; (b) Schottky junction; and (c) punch-through emitter (in normal operational condition the *p* region is depleted from carriers).

much narrower potential barrier can be obtained when other types of emitter are used. There are two well-known emitters: (1) *p-n* junction (Fig. 9.10a); and (2) Schottky junction (Fig. 9.10b). For silicon devices *p-n* junctions have a forward voltage drop of 0.7–0.8 V while Schottky emitters have 0.2–0.3 V only. As the Schottky diode is a majority carrier device, carrier storage effect is negligible.

Another interesting emitter structure is shown in Fig. 9.10c. This emitter has all the advantages of the Schottky diode even though it is fabricated out of *p-n* junctions.

The concept of static induction devices can be used independently of the type of emitter shown in Fig. 9.10. With Schottky type and punch-through type emitters the potential barrier is much narrower and this results in faster response time and larger current gain in the bipolar mode of operation.

9.6 Static Induction Diode (SID)

The bipolar mode of operation of SIT also can be used to obtain diodes with low forward voltage drop and negligible carrier storage effect [2, 5, 13, 23, 24]. A static induction diode can be obtained by shorting a gate to the emitter of the static induction transistor. Such a diode has all the advantages of a static induction transistor such as thermal stability and short switching time. The cross section of such a diode is shown in Fig. 9.11.

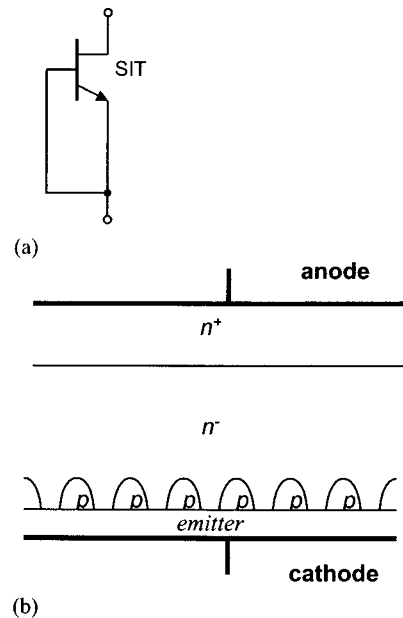


FIGURE 9.11 Static induction diode: (a) circuit diagram; and (b) cross section.

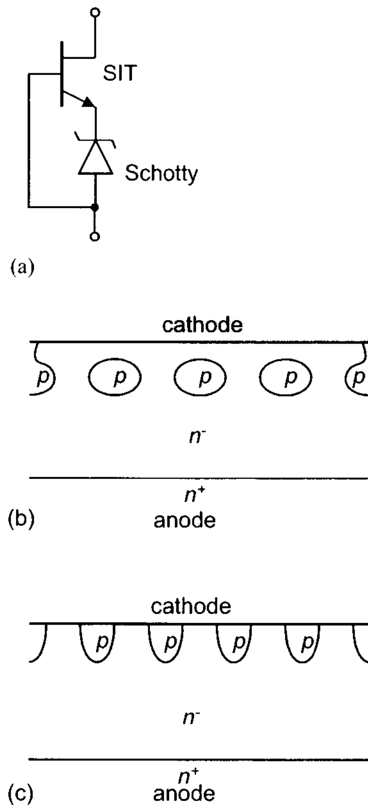


FIGURE 9.12 Schottky diode with enlarged breakdown voltages: (a) circuit diagram; and (b) and (c) two cross-sections of possible implementation.

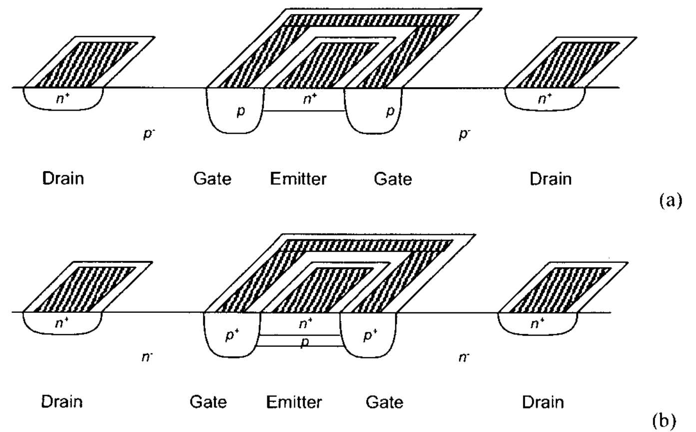


FIGURE 9.13 Structures of the lateral punch-through transistors: (a) simple; and (b) with sharper potential barrier.

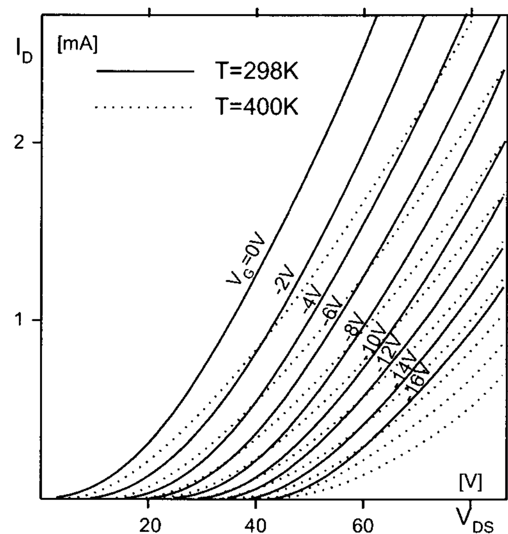


FIGURE 9.14 Characteristics of lateral punch-through transistor.

The quality of the static induction diode can be further improved with more sophisticated emitters (Fig. 9.10b,c). The SI diode with Schottky emitter was described by Wilamowski in 1983 [17] (Fig. 9.12). A similar structure was later described by Baliga [1].

9.7 Lateral Punch-Through Transistor (LPTT)

Fabrications of SI transistors usually require very sophisticated technology. It is much simpler to fabricate a lateral punch-through transistor, which operates on the same principle and has similar characteristics [15]. The LPTT cross section is shown in Fig. 9.13 and its characteristics are shown in Fig. 9.14.

9.8 Static Induction Transistor Logic (SITL)

The static induction transistor logic (SITL) was proposed by Nishizawa and Wilamowski [8, 9]. This logic circuit has almost 100 times better power-delay product than its I^2L competitor. Such a great improvement of the power-delay product is possible because the SITL structure has a significantly smaller junction parasitic capacitance and voltage swing is reduced. Figures 9.15 and 9.16 illustrate the concept of SITL. Measured characteristics of the n-channel transistor of the static induction logic are shown in Fig. 9.17.

9.9 BJT Saturation Protected by SIT

The SI transistor also can be used instead of a Schottky diode to protect a bipolar junction transistor against saturation [20]. This leads to faster switching time. The concept is shown in Figs. 9.18 and 9.19. Note that this approach is advantageous to the solution with Schottky diode because it does not require additional area on a chip and does not introduce additional capacitance between the base and the collector. The base

FIGURE 9.15 Cross section of SIT logic.

FIGURE 9.16 Diagram of SIT logic.

FIGURE 9.17 Measured characteristic of an n-channel transistor of the logic circuit of Fig. 9.16.

FIGURE 9.18 Protection of a bipolar transistor against deep saturation: (a) using a Schottky diode; and (b) using SIT.

FIGURE 9.19 Cross sections of bipolar transistors protected against deep saturation using SIT.

collector capacitance is always enlarged by the Miller effect and this leads to slower switching in the case of the solution with the Schottky diode.

9.10 Static Induction MOS Transistor (SIMOS)

The punch-through transistor with MOS controlled gate was described in 1983 [18, 19]. In the structure in Fig. 9.20a current can flow in a similar fashion as in the lateral punch-through transistor [15]. In this mode of operation, carriers are moving far from the surface with a velocity close to saturation. The real advantage of such a structure is the very low gate capacitance.

Another implementation of SIMOS is shown in Fig. 9.21. The buried p^+-layer is connected to the substrate, which has a

FIGURE 9.20 MOS-controlled punch-through transistor: (a) transistor in the punch-through mode for the negative gate potential; and (b) transistor in the on-state for the positive gate potential.

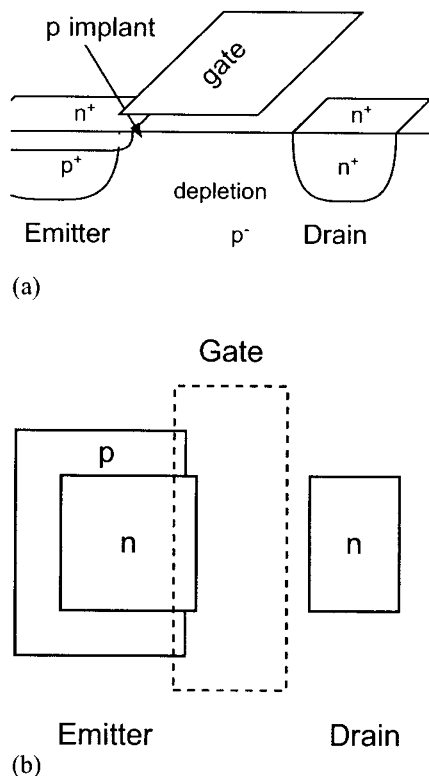


FIGURE 9.21 Static induction MOS structure: (a) cross section; and (b) top view.

large negative potential. As a result the potential barrier is high and the emitter-drain current cannot flow. The punch-through current may start to flow when the positive voltage is applied to the gate and in this way the potential barrier is lowered. The *p*-implant layer is depleted and due to the high horizontal electrical field under the gate there is no charge accumulation under this gate. Such a transistor has several advantages over the traditional MOS are:

1. The gate capacitance is very small because there is no accumulation layer under the gate;
2. carriers are moving with a velocity close to saturation velocity; and
3. much lower substrate doping and the existing depletion layer lead to much smaller drain capacitance.

The device operates in a similar fashion as the MOS transistor in subthreshold conditions, but this process occurs at much higher current levels. Such a "bipolar mode" of operation may have many advantages in VLSI applications.

9.11 Space-Charge Limiting Load (SCLL)

Using the concept of the space-charge limited current flow (see Fig. 9.22), it is possible to fabricate very large resistors on a very small area. Moreover, these resistors have a very small

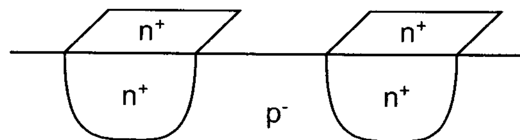


FIGURE 9.22 Space-charge limiting load (SCLL).

parasitic capacitance. The 50-kΩ resistor requires only several square μm using 2-μm technology [22].

Depending upon the value of the electric field, the device current is described by the following two equations. For a small electrical field $v(x) = \mu E(x)$

$$I_{DS} = \frac{9}{8} V_{DS}^2 \mu \varepsilon_{Si} \varepsilon_0 \frac{A}{L^3} \tag{9.17}$$

and for a large electrical field $v(x) = \text{const}$,

$$I_{DS} = 2 V_{DS} v_{\text{sat}} \varepsilon_{Si} \varepsilon_0 \frac{A}{L^2} \tag{9.18}$$

Moreover, these resistors, which are based on the space-charge limit flow, have a very small parasitic capacitance.

9.12 Power MOS Transistors

Power MOS transistors are being used for fast switching power supplies and for switching power converters. They can be driven with relatively small power and switching frequencies could be very high. High switching frequencies lead to compact circuit implementations with small inductors and small capacitances. Basically only two technologies (VMOS and DMOS) are used for power MOS devices as shown in Figs. 9.23 and 9.24, respectively.

A more popular structure is the DMOS shown in Fig. 9.24. This structure also uses the static induction transistor concept. Note that for large drain voltages the *n*-region is depleted from carriers and the statically induced electrical field in the vicinity of the virtual drain is significantly reduced. As a result, this transistor may withstand much larger drain voltages and the effect of channel length modulation also is significantly reduced. The latter effect leads to larger output resistances of the transistor. Therefore, the drain current is less sensitive to

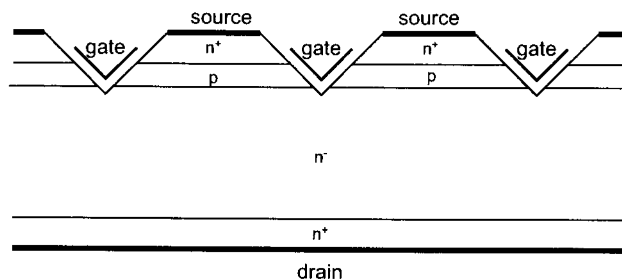


FIGURE 9.23 Cross section of the VMOS transistor.

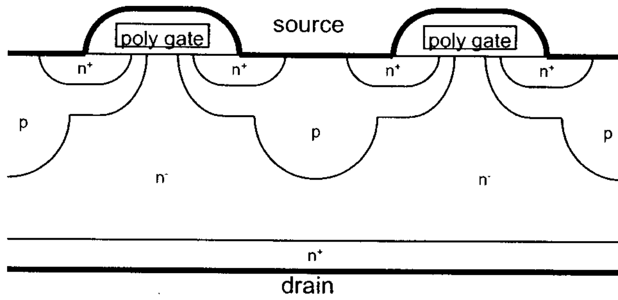
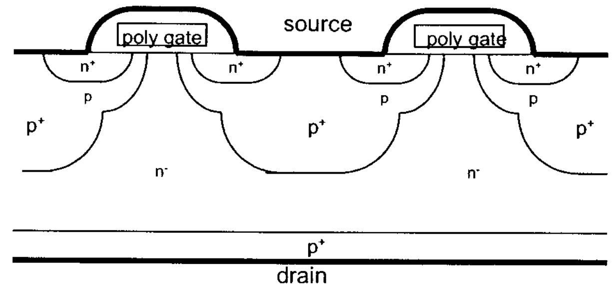
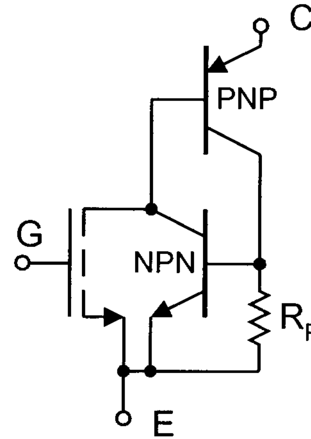


FIGURE 9.24 Cross section of the DMOS transistor.



(a)



(b)

FIGURE 9.26 Insulated gate bipolar transistor (IGBT): (a) cross section; and (b) equivalent diagram.

drain voltage variations. The structure in Fig. 9.24 can be considered as a composite of the MOS transistor and the SIT transistor as it is shown in Fig. 9.25.

The major disadvantage of power MOS transistors is their relatively large drain series resistance and much smaller transconductance in comparison to bipolar transistors. Both of these parameters can be improved dramatically by a simple change of the type of drain. In the case of an *n*-channel device, this change would be from an *n*-type to a *p*-type. This way, the integrated structure being built has a diagram of a MOS transistor integrated with a bipolar transistor. Such a structure has β times larger transconductance (β is the current gain of a bipolar transistor) and much smaller series resistance due to the conductivity modulation effect caused by holes injected into the lightly doped drain region. Such devices are known as insulated gate bipolar transistors (IGBT) as shown in Fig. 9.26. Their main disadvantage is that of large switching time limited primarily by the poor switching performance of the bipolar transistor. Another difficulty is related to a possible latch-up action of four layer $n^+pn^-p^+$-structure. This undesirable effect could be suppressed by using a heavily doped p^+-region in the base of the *npn* structure, which leads to significant reduction of the current gain of this parasitic transistor. The gain of the *pnp* transistor must be kept large so that the transconductance of the entire device is also large. The IGBTs have breakdown voltages of up to 1500 V and turn-off times in the range of 0.1 to 0.5 μs. They may operate with currents >100 A with a forward voltage drop of ≈3 V.

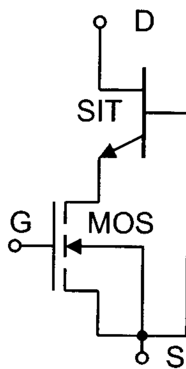


FIGURE 9.25 Equivalent diagram with MOS and SI transistors of the structure of Fig. 9.24.

9.13 Static Induction Thyristor

There are several special semiconductor devices dedicated to high-power applications. The most popular is a thyristor known as the silicon control rectifier (SCR). This device has a four-layer structure (Fig 9.27a) and it can be considered as two transistors *npn* and *pnp* connected as shown in Fig. 9.27b.

In a normal mode of operation (the anode has positive potential) only one junction is reverse biased and it can be represented by capacitance *C*. A spike of anode voltage can therefore get through capacitor *C* and it can trigger SRC. This behavior is not acceptable in practical application and therefore as Fig. 9.28 shows a different device structure is being used. Note that shorting the gate to the cathode by resistor *R* makes it much more difficult to trigger the *npn* transistor by spike of anode voltage. This way, rapid anode voltage changes are not able to trigger a thyristor. Therefore, this structure has a very large dV/dt parameter. At the same time, much energy

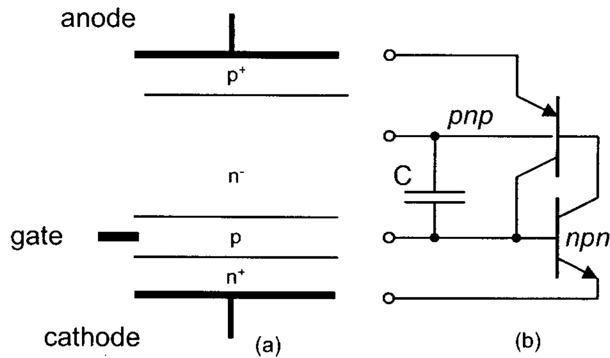


FIGURE 9.27 Silicon control rectifier (SCR): (a) cross section; and (b) equivalent diagram.

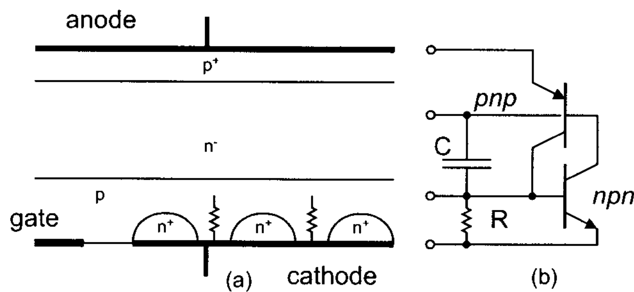


FIGURE 9.28 Silicon control rectifier (SCR) with larger dV/dt parameter: (a) cross section; and (b) equivalent diagram.

is required to trigger the thyristor with the gate signal, which is an undesirable effect and switching on time (described by the di/dt parameter) is lengthy.

Most of the SCRs sold on the market consist of an integrated structure composed of two or more thyristors. This structure has both large dV/dt and di/dt parameters. This structure consists of an internal thyristor, which significantly amplifies the gate signal.

One can notice that the classical thyristor as shown in Fig. 9.27 can be turned off by the gate voltage while the integrated SCR shown in Fig. 9.29 can only be turned off by reducing anode current to zero. Most of the SCRs sold on the market have an integrated structure composed of two or more thyristors. This structure has both large dV/dt and di/dt parameters.

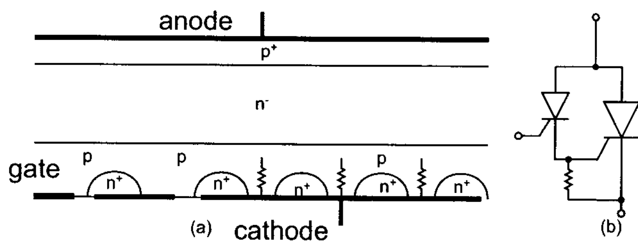


FIGURE 9.29 Integrated structure of silicon control rectifier: (a) cross section; and (b) equivalent diagram.

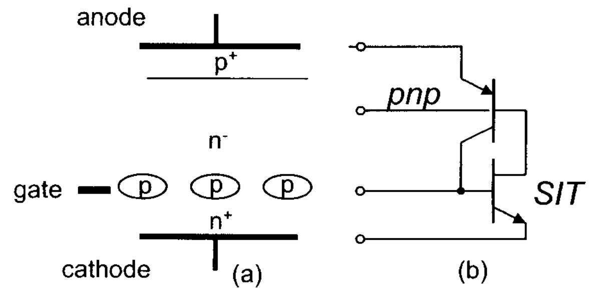


FIGURE 9.30 The GTO SITh: (a) cross section; and (b) equivalent diagram.

9.14 Gate Turn-Off Thyristor (GTO)

For dc operation it is important to have a thyristor that can be turned off by the gate voltage. Such a thyristor has a structure similar to that shown in Fig. 9.27. It is important, however, to have significantly different current gains β for *pnp* and *npn* transistors. The current gain of an *npn* transistor should be as large as possible and the current gain of a *pnp* transistor should be small. The product of β_{npn} and β_{pnp} should be larger than unity. This can be easily implemented using the SI structure as shown in Fig. 9.30.

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