A. What did you learn from this project?
I learned about the tradeoff (which datapath to use, advantages for that choice, alternative choices) and intuition that which choice seems to work great. I also learned about timing, working with ModelSim environment, and fundamental knowledge to design a processor. Starting from designing ISA and datapath to connecting all the components, I learned each component’s roles.

B. What would you do differently next time?
I would try more complex datapath. Also, when I was doing the first part of the project, I would set up the ModelSim or Xilinx ISE environment, which I spent some time, as it was reset after the new semester began. I also want to try pipelining since it is more efficient than multicycle datapath. For combined design (pipelined multicycle), it will be an interesting project as well.

C. What is your advice to someone who is going to work on a similar project?
I would advise that reviewing VHDL (either from 4200 course or from online tutorial) will be extremely helpful. In addition, I personally prefer working with ModelSim (using Linux server) than Xilinx ISE since the simulation and debugging are easier. During the course of implementation, I once tried Xilinx ISE, and because of unresolved error for simulation, I did on ModelSim, and it worked perfectly fine. Another advice is to start early and do each part at least a week before the deadline. For people doing the project alone, I would advise them to choose a simple datapath.