CPU Design Project – Part 6
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(a) What did you learn from this project?
This project helped us learn Verilog and get familiarized to the tools Modelsim and Quartus II. Most importantly, it helped us understand how to design a CPU from scratch using Verilog (Instruction Set Architecture, Datapath, Verilog Modeling), how to use Verilog modeling and simulating tools better, and how to work with the Altera DE2 FPGA.
What is more, we’ve learned that simulation is not everything. You may get a right result on simulation but it still needs way more time to deal with the timing problems which are going to occur on the board.

(b) What would you do differently next time?
In case we redo the project, we will try to implement it with a pipeline datapath which would offer improvements over a multicycle architecture. Also, adding another ALU so that some instructions (BEQ, BNE) can require less clock cycles. Besides, we would like to design a better ISA, so that it would be more convenient for us to design the datapath and control unit. It also can be a challenge to try a multi-processor system.

(c) What is your advice to someone who is going to work on a similar project?
It is better to start the project early and meet all the time lines as they are designed to complete the project in the right time. It is good to test each component in the board after simulating it. It could help to verify the simulation of the control signals and each and every component in the datapath. The startup could be time-consuming, especially if you haven’t worked on VHDL or Verilog before. But the project is really interesting at the end(Well, the fun may only occur when you finally finished the project). By the way, I’ll say it another time, leave more time for the board work, simulation is not the finishing line.
Also, I recommend every one of you to use the board as fast as you can, if you can run each component independently on the board it will be much easier for the final implementation.