What did you learn from this project?

Designing a CPU in this project improved my understanding and appreciation for VHDL. It also made me more appreciative of Simulation tools such as ModelSim. I would say the most I took from this is accurate and complete simulations. Verifying the design is the most important thing in this project.

What would you do differently next time?

Start the design process earlier. The problems encountered can only be solved with having enough time to debug the issues. There will be many timing issues and these were only solved through trial and error.

What is your advice to someone who is going to work on a similar project?

Do not take this class in conjunction with senior design. The senior design project will most likely take up the majority of the time you have in the week to work on other classes. Get a board early and start trying to synthesize the design early in the project. This way at the end you will have at least some of the design implemented if you are unable to implement it all. And above all make sure that the design is verified well in simulation. If one part is wrong you will spend the majority of your time fixing earlier parts than working on later parts.