What did you learn from this project?

The project taught us designing and implementing CPU designs. We worked on the tools like ModelSim, Quartus and used Altera FPGA Boards in part 5. We now understand the different steps involved in designing a multi-cycle datapath. In the final step of the project, we learned how to simulate our processor on the Altera FPGA board provided in the lab.

What would you do differently next time?

We would probably try to create an instruction set closer to the MIPS instructions so that debugging and troubleshooting might be easier during development. We would give ourselves more time to write more simple programs on the FPGA for testing and to get more familiar with tools, Quartus II especially. Further, we would be more involved in assigning pins to our signals for implementation on the DE2 board. That proved to be the biggest challenge for us.

What is your advice to someone who is going to work on a similar project?

We would like to recommend future students to start the project as early as possible. The project may look straightforward but one should not wait until the last minute as it becomes tricky in the later parts. For debugging, one needs to thoroughly check each component in the datapath one by one which is time consuming. We would suggest that students, who prefer to implement the multi-cycle datapath, to do the datapath verification part along with the Control Unit part. This would help them verify their datapath successfully. Verification of the datapath after designing the control unit becomes much simpler. One should start to work with the Altera Quartus tool as soon as possible, as it brings on a lot of issues to be resolved.