CPU Design Project Part 6 Report
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I. What did I learn

The project is about how to design a CPU. During this project, I know the exact structure of inner of the CPU. It also makes me know more about the principles of instruction set and how to design a data path. It is also the first time for me to learn VHDL language.

II. What would I do different next time

I may choose to design different data-path, especially the pipeline data-path, which would help me understand better about the hazard.

This time I design a normal state table but when I try to program I find it is also some kind of complicated. So I may also try to simplify the state table to make the program execute faster.

Also, I will try to learn more about the VHDL because I only know a little about VHDL now and I cannot use VHDL to design something complicated.

III. My advice to the one who is going for this project

I am my only person in my group. So I will tell him he should design as simple as possible because it will take much time to achieve all the functions of the design.

Also, I am my only person in my group. But I still want to tell him try to do that all by himself. Although it will take him much more time and sometimes he may be fretful, he will learn all the details in the CPU and every fault during the debugging will be a challenge and a gain for him.