What did you learn from this project?

The fact that we had designed and implemented a CPU has been a great learning experience. Starting with project we had basic knowledge of the VHDL language, but the project helped us to become more familiar with the language. We also had to work on tools like Modelsim, Quartus and also programming on Altera FPGA Boards, this has given us an in-depth understanding of how the tools work. We now understand the different steps involved in designing a multi-cycle datapath. In the final step of the project, we learned how to simulate our processor on the Altera FPGA board provided in the lab and how to use the ‘In-System Memory’ tools to run our test program straight from the Quartus software. One thing which the project taught us is to believe in ourselves and work hard.

What would you do differently next time?

We would work to make our design more simpler, because we ran into a lot complexities due to our complex design, we understand that simpler the design, more is the efficiency.

We would also start off working with the Altera Quartus tools as soon as possible, so that we can resolve the errors created while running the code on the board. For instance, we faced problems while executing the branch and jump instructions for executing loops. Individually the two instructions were working fine, and there were no errors in the ModelSim simulations, but we could not make them work in the Quartus II tool. The problem was related to the updating of the program counter. Also next time we would be aggressive to take up the challenge of implementing the Pipelined Datapath incorporating the Hazard Detection and Forwarding unit.

What is your advice to someone who is going to work on a similar project?

Don’t Panic looking at the Project, we suggest that you take up each part by itself, and work regularly, as you start working on it, you will be able to connect the dots. At the End, for debugging, one needs to thoroughly check each component in the datapath one by one which is time consuming, so verifying of the datapath after designing the control unit makes it simpler. Ask, the T.A for any help regarding the project, he/she can be of great help.

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