What did I learn from this project?

By doing this project, I’ve gained a much better understanding of how instruction sets and processor architectures are designed. I’ve learned in detail exactly how the typical single-cycle, multi-cycle, and pipelined data-paths work. I’ve also gained more hands-on experience modeling hardware using VHDL, simulating it using ModelSim, and deploying it to an FPGA.

What would I do differently next time?

I’m pretty happy with the way I designed and implemented my processor. If I were to create another multi-cycle processor, I don’t think I would really make any significant design changes. I would however, add a few things to my current design such as more addressing modes for my MOV instruction. Multiply, divide, and shift instructions would be nice additions too.

Or I might give a pipelined processor a shot if I were to do this project again.

What is my advice to someone who is going to work on a similar project?

Make sure you have a good design before you start working on the VHDL, including bit templates for all of the instructions, and a detailed data-path diagram.