Tuesday, 1/28/25

Techniques to Reduce Recombination

(1) Create a Back Surface Field (BSF)

Make a heavily doped Al layer at the backside of the device (in the p-type) layer). This helps to capture red photons (which go deeper into the Si), and it serves as the backside electrical contact.

The heavier p++ doping sort of acts like a pn junction with the p+ doping closer to the MJ, helping to push free electrons toward and across the MJ to the n-type Si.

(2) Passivate the bare Si sides and tops with SiO_2

A thin layer of passivating oxide reduces dangling Si bonds to reduce recombination here.

(3) Add near-the-top contacts

In the n-type layer.

Heavily dope (n++) to create "minority carrier mirrors," to dissuade holes in the n-type layer from approaching the metal contacts and recombining with free electrons. Similar in operation to the BSF with electrons.

Optical Losses and Minimizing Them

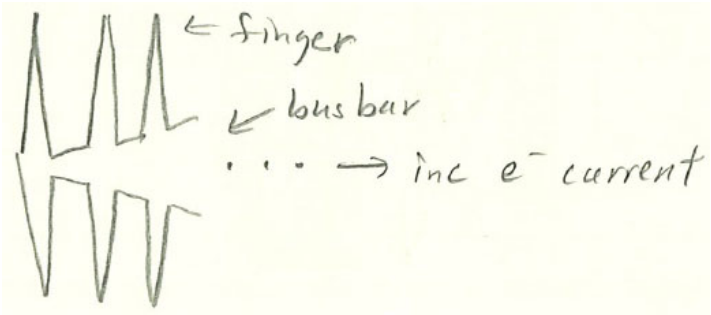
(1) Shadowing of the top contacts

The metal top contacts block photons from entering the Si.

a. To minimize this, make them as narrow as possible.

Unfortunately, their resistance (and therefore resistive losses) increases as the top contact fingers' area decreases.

b. Taper the top contact fingers and the associated busbars so that their widths increase with increasing current:



c. Contact resistance at the metal-semiconductor interface

In addition to resistance to current flow in the finger and busbar structure, there is the contact resistance between the metal and the Si.

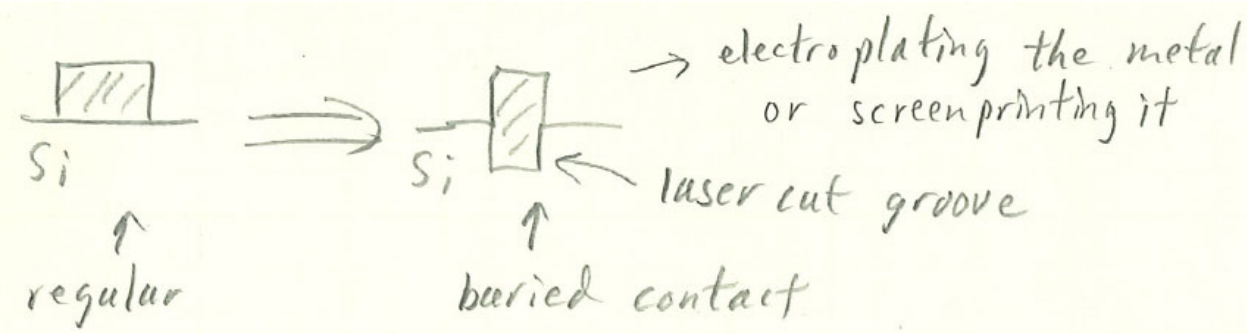
This can be reduced by heavy doping of the top layer of the semiconductor.

Trade off: this heavy doping can create a "dead zone" in the top layer of the semiconductor which reduces the collection efficiency of blue photons (higher energy photons: absorbed close to the cell's top surface.)

d. Buried contact solar cells

The typical loss due to contact shading is approximately 8% to 12%.

Buried contact solar cells maintain finger/busbar cross-sectional area by laser forming grooves in the top surface of the Si and the deposing the metal up vertically:



(2) Si's indirect semiconductor properties

Blue photons (higher energy photons) are absorbed close to the cell's top surface.

Red photons (lower energy photons) must travel much further in the Si to be absorbed. The optimal Si thickness would be > 1 mm.

Trade off: electron-hole pairs created far from the SCR (depletion region) often experience recombination.

So, if the cell thickness is approximately 200 μm, longer wavelength photons may travel out of the back of the cell before generating an electron-hole pair.

Light trapping techniques may be employed to increase the path length of long wavelength photons in the Si cell.

> Example: roughening the backside to reflect light in random directions to increase pathlength.

(3) Top surface optical reflection

Some of the photons reflect off of the top surface of the PV cell and are not captured. Several techniques can be used to reduce this:

a. Antireflection coatings (ARC)

ARCs can be applied to the top Si surface.

They use a 1/4 wavelength ARC thickness so that the reflected light is 180^o out of phase at the surface at that wavelength:

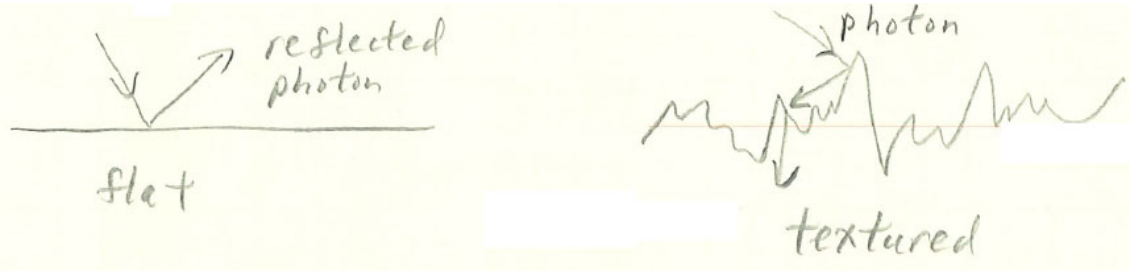
$$d = \frac{\lambda}{4n},$$

where n is the ARC coating material index of refraction.

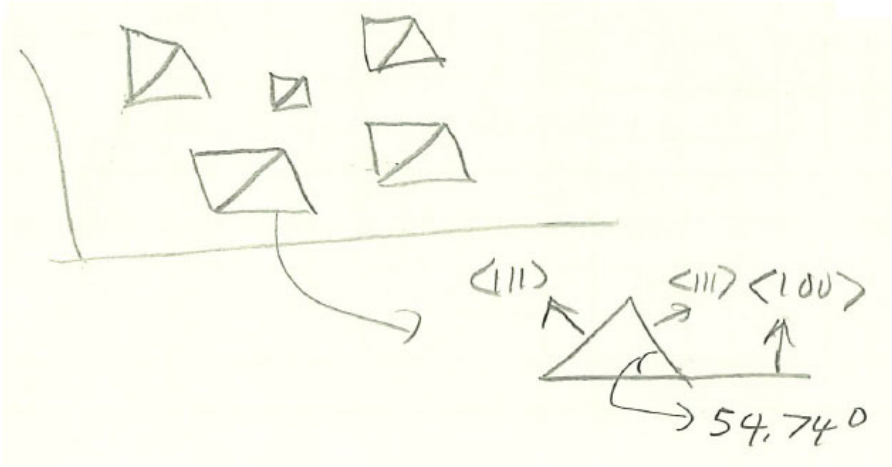
This technique only works at one wavelength. Therefore, pick λ to coincide with peak photon flux: 0.65 μm.

b. Top surface texturing

Roughen the top surface to encourage reflections into Si islands on the surface:



(100) Si can be anisotropically etched to create tiny 4-sided pyramids called hillocks:



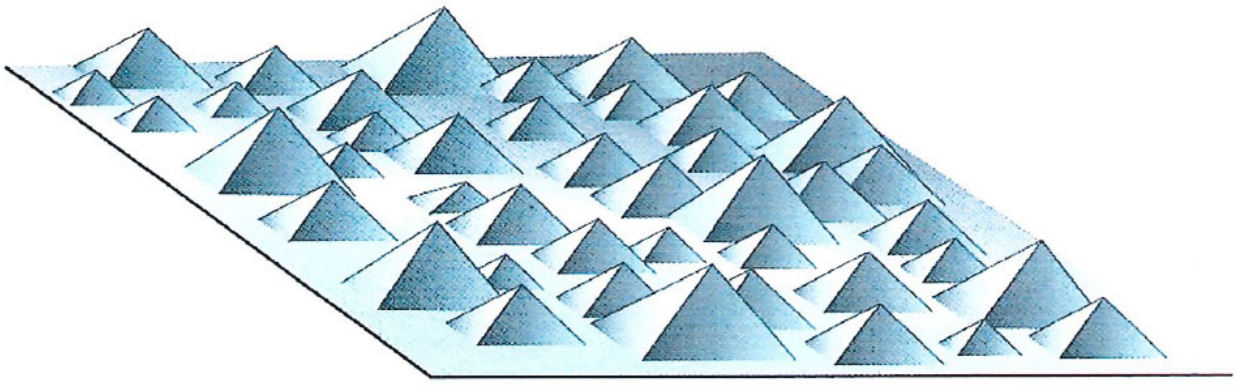


Figure 2.18 Texturisation by raised pyramids.

Quantum Efficiency

If photon energy < E_G: no electron-hole pair is created.

If photon energy = E_G: an electron-hole pair is created.

If photon energy > E_G: an electron-hole pair is created and waste heat is produced.

Therefore, the maximum quantum efficiency in a Si a solar cell is about 33% for a single junction device.

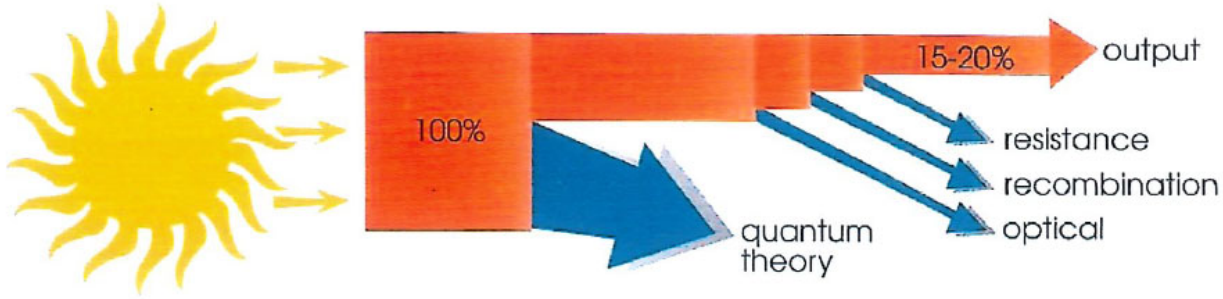
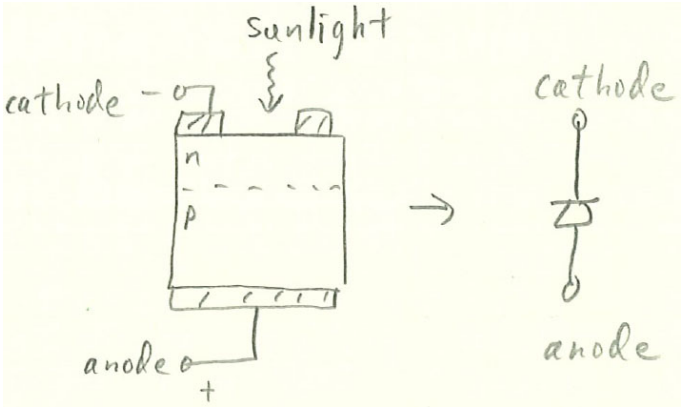


Figure 2.14 Solar cell losses.

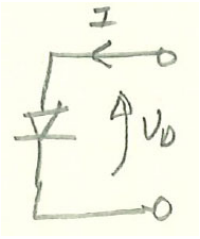
Generating Power with PV Devices

1. Review



2. PV Dark Operation

Current flows into the anode like a normal pn junction diode:

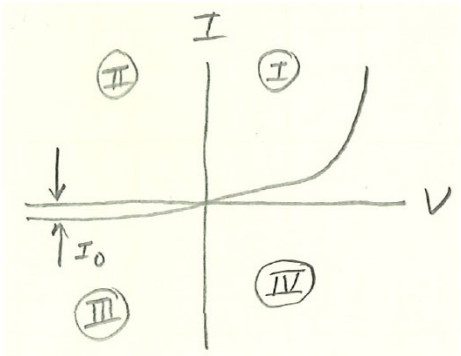


$$I = I_D = I_o\left(e^{\frac{qV_D}{KT}} - 1\right) = I_o\left(e^{\frac{V_D}{V_T}} - 1\right),$$

where I_o is the reverse saturation current. This is the standard forward operating equation for a pn junction diode. Note: I_o is called I_s in the electronics world…

In this mode, the PV device is a <u>power dissipating load</u> to an external voltage source (such as a rechargeable battery).

If we plot I and V for the PV device operating in the dark, we get the following performance graph:

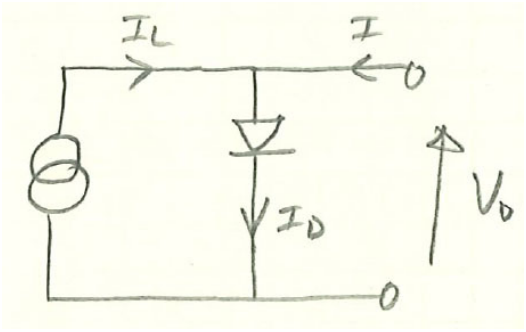


Observe that the PV device (just like a normal pn junction diode) operates in the 1st quadrant (forward bias operation) and 3rd quadrant (reverse bias operation) only.

In Quadrant I: I and V are positive. In Quadrant III: I and V are negative.

3. PV Operation in Light

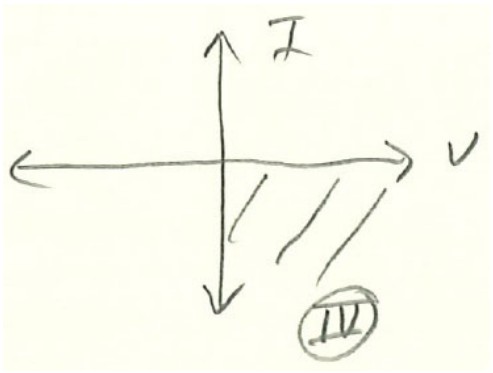
Our PV device can be modeled as:



Which is a current source in parallel with a pn junction diode:

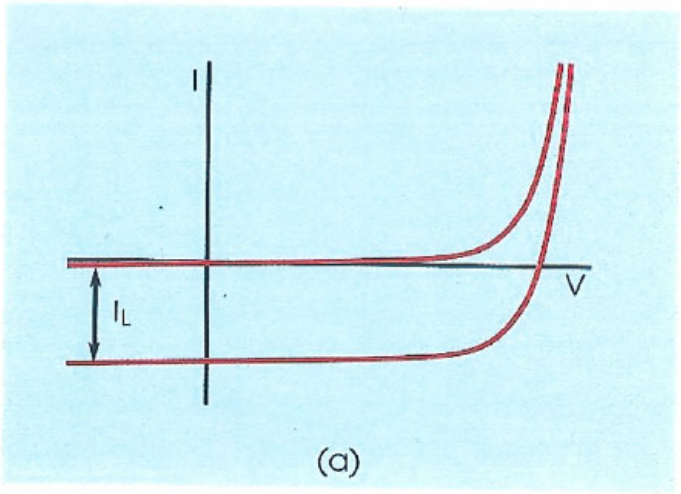
$$I = I_o\left(e^{\frac{V_D}{V_T}} - 1\right) - I_L.$$

Here, I < 0 A and V > 0V → operation in Quadrant IV:



Usually, they flip the graph over about the x-axis so that Quadrant IV → Quadrant I.

This yields a plot of V vs. –I. Consider the example below from the textbook:



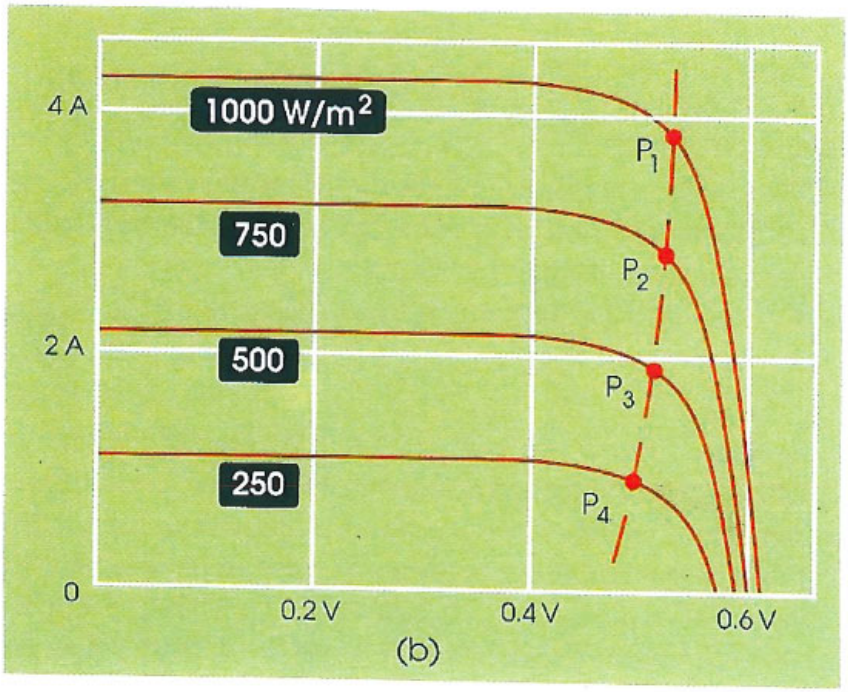


Figure 2.10 (a) The light-generated current shifts the cell's characteristic into the fourth quadrant; (b) a family of *I–V* curves for a 2 W_p solar cell.

Fig. 2.10 illustrates a family of performance curves for a monocrystalline Si PV cell rated by the manufacturer at 2 W_p.

Each curve represents a different strength of sunlight (insolation level).

The normal rating for W_p (Peak Watts) is when the PV cell is exposed to "standard conditions": 1000 W/m^2 insolation, at 25°C, AM1.5 solar spectrum.

$V_{OUT_{max}}$ → open circuit voltage (V_{oc}): I = 0 A and P = 0 W.

$I_{OUT_{max}}$ → short circuit condition (I_{sc}): V = 0 V and P = 0 W.

MPP → Maximum Power Point → occurs at a V slightly less than $V_{OUT_{max}}$ and an I slightly less than $I_{OUT_{max}}$.

Notice that MPP moves as the insolation varies. This necessitates the use of an instrument called a Maximum Power Point Tracker if maximum power is to be obtained from the PV cell over a wide insolation range.

Observe that $V_{OUT_{max}}$ is approximately 0.6 V, which is less than the nominal voltage for a typical dry cell battery, 1.5 V. Therefore, PV cells are usually connected in series to increase the system output voltage, and then these units are connected in parallel to increase the system output current.

A standard battery approximates an ideal voltage source: fixed V, variable I. However, a PV cell approximates an ideal current source: fixed I, variable V.

Notice that V_{oc} is approximately 0.6 V regardless of insolation. 0.6 V is about the forward turn-on voltage for a pn junction diode.

Notice that I_{sc} varies in proportion to the insolation. I_{sc} is also approximately proportional to the PV cell's surface area.

a. Fill Factor

Fill Factor (FF) is a widely used measure of performance for PV cells. Consider Fig 2.11:

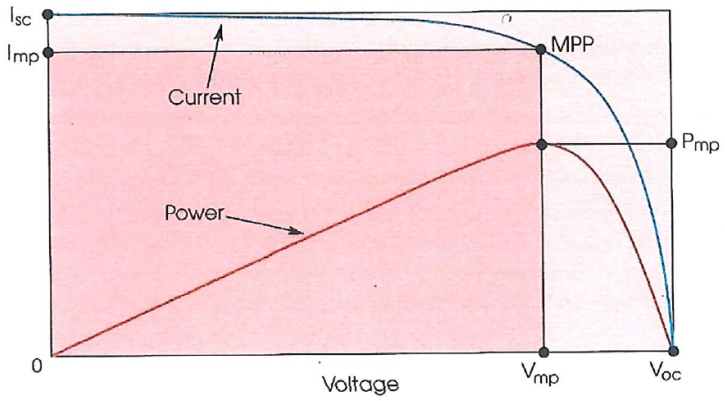


Figure 2.11 *Current and power at standard insolation.*

Fill Factor can be computed by: $FF = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}}$.

For an "ideal PV cell": $I_{mp} = I_{sc}$ and $V_{mp} = V_{oc} \rightarrow FF = 1$ or 100% fill.

For practical PV cells: FF ~ 70%.

4. Temperature Effects

V_{oc} decreases as the operating temperature increases: approximately 0.33% per °C for monocrystalline Si PV cells.

Therefore, PV cells have a <u>negative</u> temperature coefficient.

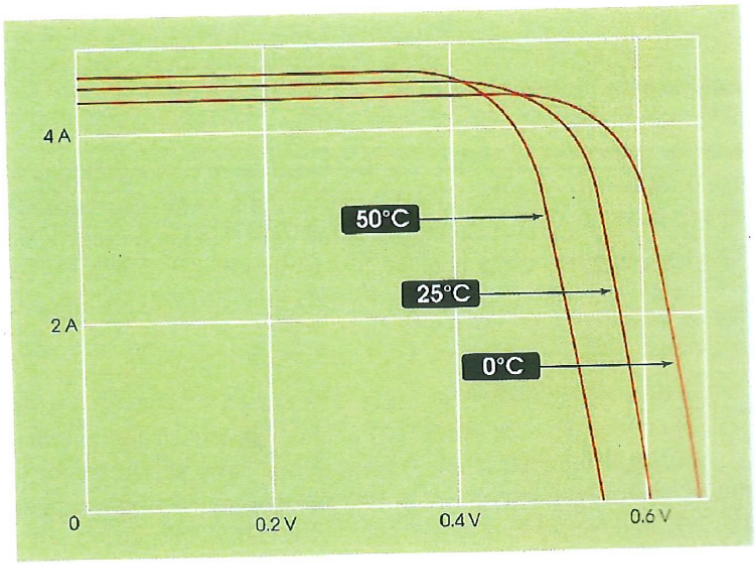


Figure 2.12 Effects of temperature on the *I–V* characteristic.

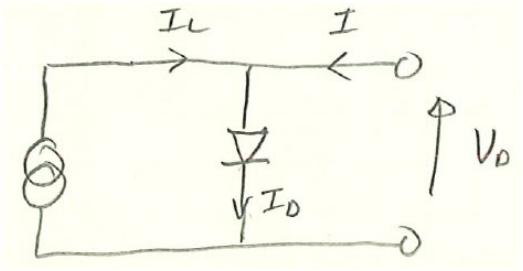
Observe that although I_{sc} increases as the operating temperature increases, it increases much less that V_{oc} decreases. Therefore, power output <u>decreases</u> as temperature <u>increases</u>.

Note: winter in northern latitudes with sunny days where snow cover reflects light onto a PV array is a good application for PV.

In hot climates, PV cells may reach 70°C → techniques for cooling them are important in these conditions.

5. Modeling Resistive Losses in the PV Cell

a. Let's reinvestigate the PV circuit model:



$$I = I_D - I_L = I_o\left(e^{\frac{V_D}{V_T}} - 1\right) - I_L.$$

For $I_{sc} \rightarrow V_D = 0$ V : $I_D = 0$ A

Therefore $I = -I_L = -I_{sc}$.

Therefore $I_L = I_{sc}$.

For $V_{oc} \rightarrow I = 0$ A and $I_L = I_D = I_{sc}$.

Therefore $I_{sc} = I_D = I_o\left(e^{\frac{V_{oc}}{V_T}} - 1\right)$

Rearranging: $V_{oc} = V_T ln\left(\frac{I_{sc}}{I_o} + 1\right)$.

I_{sc} is defined as the "light current" and I_o is defined as the "dark current."

Therefore V_{oc} is a function of light and dark currents.

If we include the diode nonideality factor, n: $V_{oc} = nV_T ln\left(\frac{I_{sc}}{I_o} + 1\right)$. However, n is close to 1. Note: n is often called λ in the electronics world…

Note: $V_T = \frac{KT}{q}$.

Therefore: $V_{oc} = \frac{KT}{q} ln\left(\frac{I_{sc}}{I_o} + 1\right)$, which indicates that V_{oc} increases with temperature! However, it does not!!

The dark current, I_o, <u>increases</u> with temperature, enough to offset increasing T in the equation above, so that V_{oc} <u>decreases</u> as temperature increases.

b. Modelling Losses

Consider again Fig. 2.14:

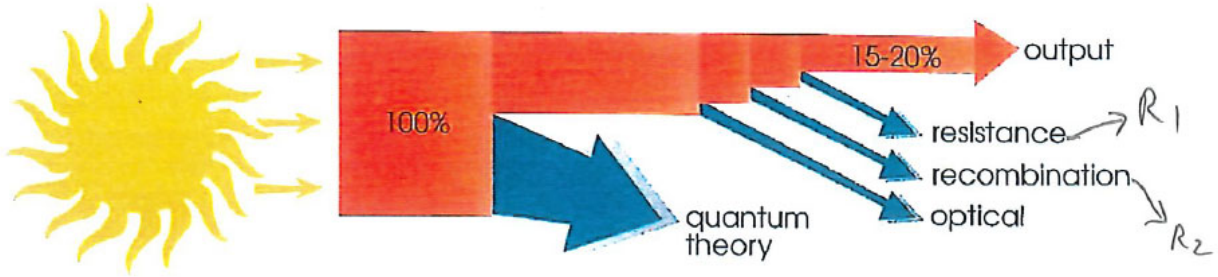
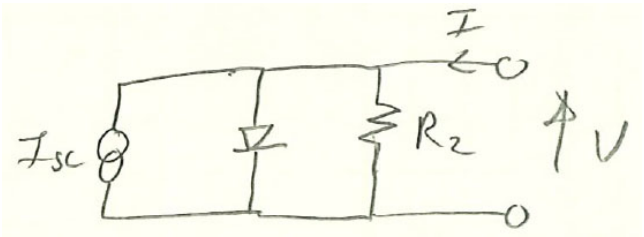


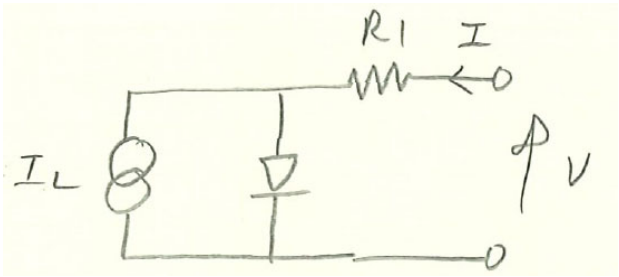
Figure 2.14 Solar cell losses.

(1) Recombination and other "shorting losses" can be modeled as a shunt resistor, R_2, in parallel with the PV device:



The effect of R_2 on PV device performance is a small decrease in V_{oc} and a larger decrease in the fill factor.

(2) Resistive losses (resistance in the contacts, bus bars, fingers, and the bulk semiconductor material) can be modeled as a resistor, R_1, in series with the PV device:



The effect of R_1 is a small decrease is I_{sc} and a larger decrease in the fill factor.

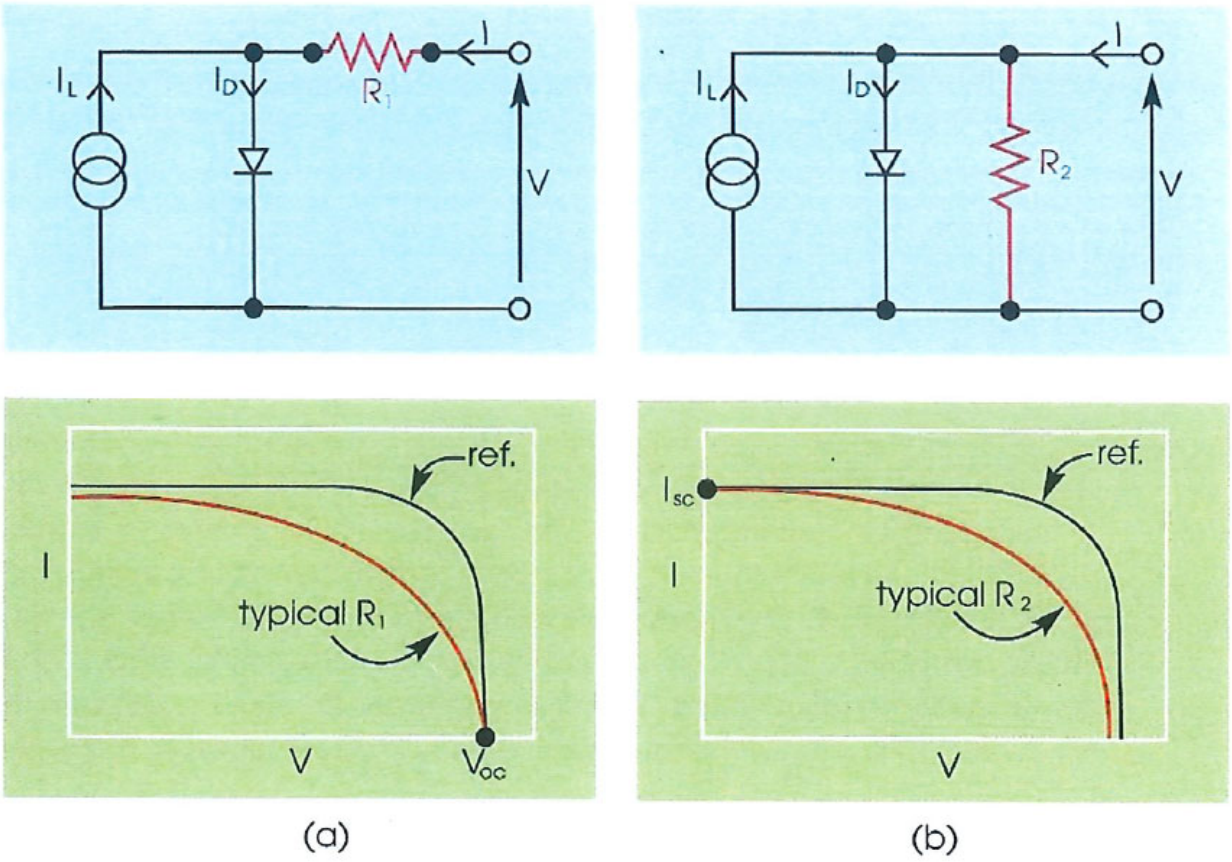
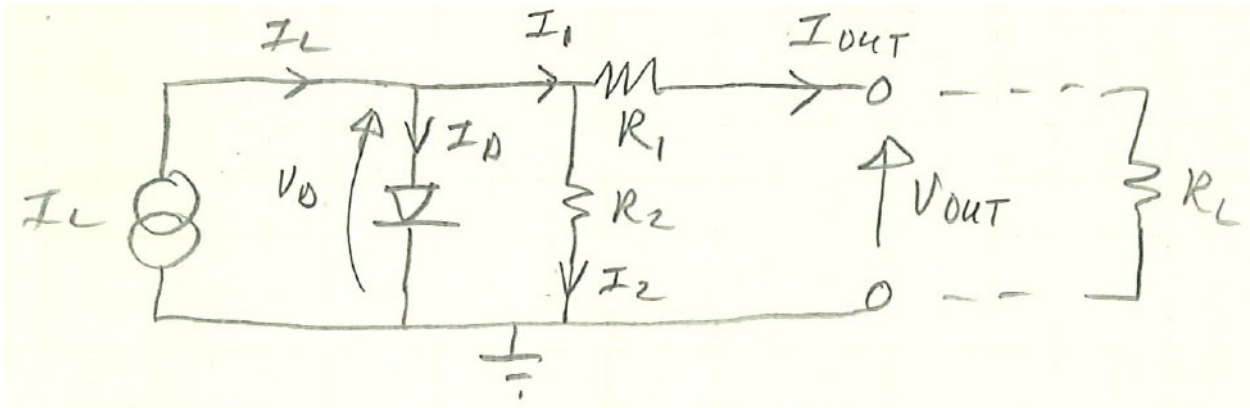


Figure 2.21 Equivalent circuits and *I–V* characteristics of a solar cell that includes: (a) series resistance; (b) shunt resistance.

(3) Consider the circuit model with both R_1 and R_2:



$$I_1 = I_L - I_D$$

$$I_D = I_o\left(e^{\frac{V_D}{V_T}} - 1\right)$$

$$V_D = V_{OUT} + I_{OUT}R_1$$

$$I_{OUT} = I_1 - I_2$$

$$I_2 = \frac{V_D}{R_2} = \frac{V_{OUT} + I_{OUT}R_1}{R_2}$$

Therefore $I_{OUT} = I_L - I_o\left(e^{\frac{V_{OUT}+I_{OUT}R_1}{V_T}} - 1\right) - \frac{V_{OUT}+I_{OUT}R_1}{R_2}$

However, due to the complexity of this equation, usually the effect of R_1 and R_2 are only considered independently.