High Sensitivity Signatures for Test and Diagnosis of Analog, Mixed-Signal and Radio-Frequency Circuits

by

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Abstract

The conventional approach, widely practiced in the industry today, for testing analog circuits is to ensure that the circuit conforms to data-sheet limits on all its specifications. However, such a specification based test methodology suffers from high levels of test cost stemming from long test-times on expensive test equipment. In recent years the situation has only worsened with the advent of mixed signal systems on chip (SoC), to a point where analog circuit test cost is often found to be as much as 50% of the total test cost in spite of analog portions occupying less than 5% of the chip area.

To alleviate the analog circuit test cost problem, a number of techniques exist in the literature that can be broadly classified as (a) fault-model based test or (b) alternate test. Fault model based test techniques direct their tests to identify faults in circuit components much like their digital circuit test counterparts resulting in a test approach that can be easily automated and relies on readily available output measurements on inexpensive test equipment. On the other hand, alternate test techniques test a circuit by building a regression model relating a few easily observable output parameters as signatures of the circuit to the actual circuit specification.

Both these test paradigms for analog circuit test, however, have limited industry acceptance due to a lack of confidence in the defect level and yield loss that the test procedures can guarantee in the face of high manufacturing process variation and low signal levels that are characteristic of modern analog circuits. An important reason for the (typically) high defect level and yield loss resulting from the use of either of these two test paradigms is the unavailability of easily obtainable circuit outputs that are (a) sufficiently sensitive to circuit component values and (b) have a high degree of correlation with circuit specifications.

The main objective of this thesis is to design analog test signatures (and associated test procedures) that are (i) sensitive enough to capture even small variations in circuit components, and (ii) sufficiently correlated to circuit specifications and yet obtainable at limited or no additional hardware and input signal design effort. Additional objectives of this thesis are to: 1) Extend the use of the new signatures to diagnose faulty circuit components in analog circuits. 2) Use the test signatures to distinguish faults resulting from defects caused by manufacturing process related variations. 3) Evaluate the theoretical bounds on the achievable defect level and the resulting yield loss of fault model based test procedures relying on these signatures.

The sensitivity of the proposed test signatures is enhanced by an exponential transformation, called V-Transform. The new test signatures and associated procedures are evaluated using three metrics test time, defect level (test escapes), and yield loss. We analyze the proposed signatures theoretically in addition to extensive computer simulations and hardware measurements on common RF/analog circuits such as filters and low noise amplifiers. A representative result of one of our experiments is as follows: For 400 low noise amplifier circuits that were tested, we find that the proposed V-transform based signatures resulted in smaller test escape ($\approx 2\%$) and yield loss ($\approx 3\%$) when compared to other prevailing alternate test or fault-model based test methods, while significantly reducing test time (by as much as 50%) compared to the traditional specification based test methods.

Acknowledgments

First and foremost, I would like to thank my advisor Prof. Vishwani D. Agrawal for encouraging me to start on this doctoral program and constantly challenging me to push the limits and seek out bold, new ideas. His enthusiasm for research and learning is infectious, which is something I hope I have picked up and would like to embody in my own life. Big thanks goes out to Prof. Adit Singh and Prof. Foster Dai for serving on my thesis committee, and in each of whose classes, I learned significant material that helped me get a good grounding in the broad areas of VLSI Design and Test. Thanks are due to Prof. Alvin Lim for serving as the external reader on my committee. I owe a debt of gratitude to Prof. Virendra Singh (IIT Bombay, India), whose early interest in my work spurred me to pursue it further, which has eventually come to be my PhD thesis. I should thank members of the analog test community, particularly Haralampos Stratigopoulos (TIMA labs, France), whose comments at various points in time have benefited this work.

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Finally, I would like to thank my extended family for being supportive of all my endeavors. This thesis is dedicated to them.

Poem by the Author

Working is tricky,

If you choose to be picky!

Research is sucky,

When you try to be finicky!

I knew this already,

But I chose to be heady.

After a while,

I've realized, it was all worthwhile!

I pushed myself to publish many papers,

Even as I wonder if they'll end up in diapers!

I hope many other folks will cite my paper,

Lest I be labeled an academic pauper!

I'm finishing this dissertation,

Without much adoration;

Oh God, my Committee,

Will they approve my Ph.D.?

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Chapter 1

Introduction

1.1 What are RF/Analog/Mixed-Signal Circuits?

"RF/Analog/Mixed-signal" is a label associated with circuits that have a portion of their operating input, or output, or both input and output, consisting of continuous-time, continuous-amplitude signals, as opposed to digital circuits that have both their operating input and output consisting of discrete-time, quantized-amplitude (Boolean) signals.

RF circuits can be broadly classified as circuits that process signals in the high-frequency (ranging from a low of 20 kHz all the way up to 60 GHz or higher) domain. Examples include low noise amplifier (LNA), mixer, filter, and voltage controlled oscillator among others.

Analog circuits are a bigger class of circuits, in that, they encompass all continuous-time, continuous-amplitude signal processing circuits. As such RF circuits can be thought of as a subset of analog circuits operating in the high-frequency range [103]. Examples include dc power supply circuits such as regulators, op-amps, and signals conditioning circuits.

Mixed-signal circuits are those that function as a bridge between the digital and the analog worlds, in that one of their operating input (output) is continuous-time, continuous-amplitude (known as analog) signal, while the output (input) is discrete-time, discrete-amplitude (known as digital) signal. Examples include analog-to-digital converters (input = analog, output = digital), and digital-to-analog converters (input = digital, output = analog). Digital circuits have both their inputs and outputs in the discrete-time discrete-amplitude domain. Figure 1.1 illustrates the input/output domain distribution of RF/analog/mixed-signal and digital circuits with example circuits for each type.

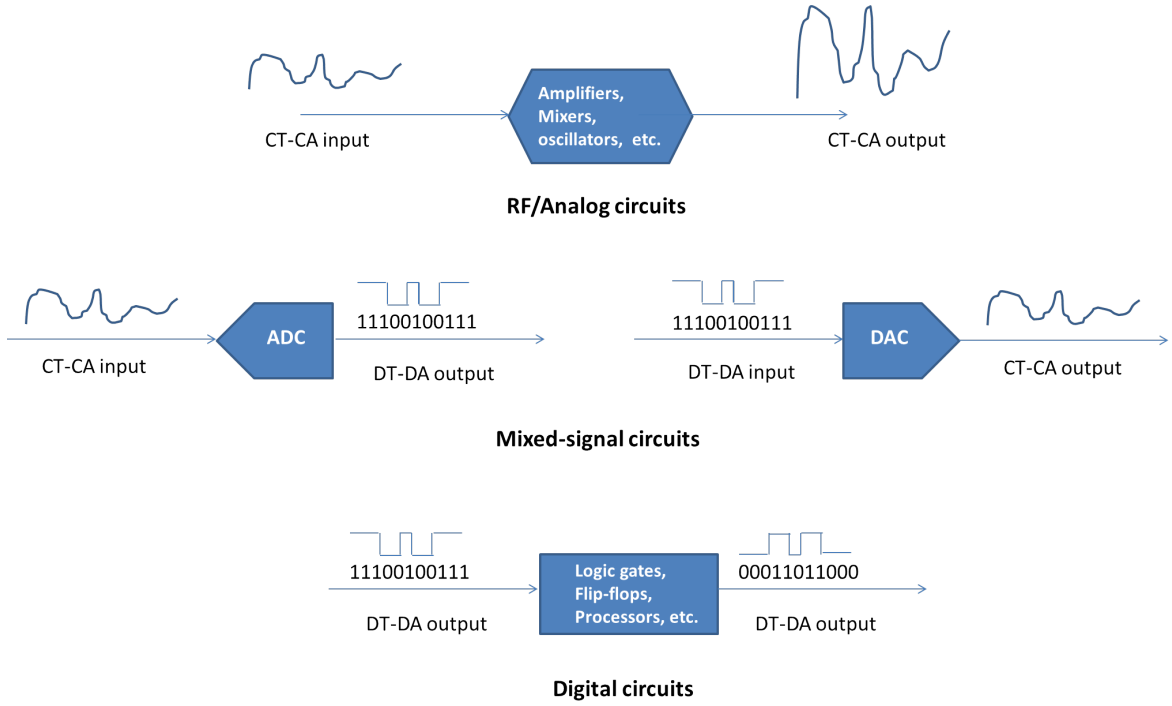


Figure 1.1: Distribution of input/output functions of different types of circuits.

1.2 Role of RF/Analog/Mixed-Signal Circuits in Today's Digital World

The nature of information produced in the world around us is analog, that is, the myriad information sources–such as sensors, be it video, audio, heat, light, or radio frequency (RF)–generate signals in a continuous-amplitude, continuous-time fashion. On the other hand, today's computing is leveraging the digital microprocessor revolution where most computation happens digitally in a large monolithic piece of silicon. Consequently, any processing of these signals calls for a bridge between the analog and digital worlds. Analog-to-digital converter (fittingly named) is a typical circuit that functions as a bridge. There are many other analog circuits needed before the signal becomes bridgeable like signal-conditioning circuits that make use of amplifiers, filters and so on.

Similarly, the radio waves transmitted in free air by today's ubiquitous cell-phones are relayed by virtue of those waves being high-frequency analog signals [74]. At the transmitting as well as the receiving end of such a wireless communication system, processing

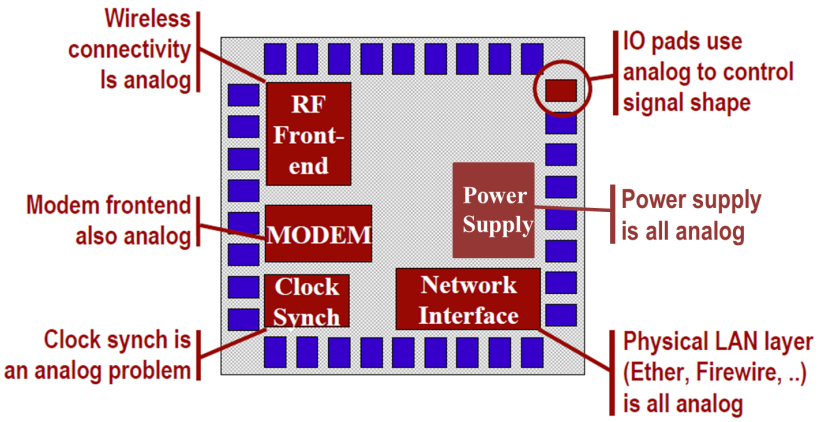


Figure 1.2: Hypothetical picture illustrating different blocks that make use of analog/RF modules in a typical RF-SoC (for mobile devices).

(coding/decoding) of radio signals is accomplished by several RF or analog circuit blocks such as low noise amplifiers, phase-locked loops, mixers, and filters [104].

Analog amplifiers are also used at the digital chip boundaries acting as buffers to drive the pins with adequate amounts of current [50]. Direct-current (dc) power-supply required to power digital or analog circuits are composed of analog circuitry. Virtually any system-on-chip (SoC) or custom integrated circuit conceivable ends up having a portion of analog circuitry for accomplishing one or more of the tasks noted above. In other words, analog is everywhere in todays digital world. Figure 1.2 shows the RF/analog circuit portions in a typical RF-SoC of today. Notice that RF/analog circuits contribute to roles from powering up the chip to enabling communication with the external world.

1.3 Analog Test Versus Digital Test

Digital circuits have succinct fault models (like the stuck-at fault) allowing the use of "structural" tests that target specific faults instead of testing for the entire functionality of the circuit. They serve as effective replacements of functional tests, thereby obviating long test times that would have otherwise been necessary for running functional tests even on a moderately-sized digital circuit. Consider for example an n-input, m-output, g-gate

digital circuit (without memory elements like flip-flops); testing such a circuit exhaustively for functionality can take 2^n vectors in the worst-case [33]. Clearly the number of vectors needed to test the circuit is exponential in the number of inputs in the circuit. On the other hand by targeting faults individually (based on a fault model), the number of test vectors needed to test the complete circuit is bounded by the number of faults to be targeted. For this example, it is of the order of $m + n + g$. Consequently, fault model based tests considerably reduce the number of test vectors needed when compared to functional tests for large digital circuits. Common structural defects (e.g., signal line short to power and/or ground rails or other signal lines) in integrated circuits are easier to model as faults in digital circuits due to the fact that the deviant behavior in the presence of a fault can be defined concisely (for example, as an incorrect logic value, of which there are only two possibilities–1 or 0) at any node in the digital circuit. This simplicity in fault-modeling is an important factor contributing to the prevalence of structural testing in digital circuits.

In contrast, analog circuits propagate signals through them in a continuum of signal values, requiring a large number of test signals to test the circuit. The deviant behavior in a faulty analog circuit can take a whole spectrum of incorrect values. For example, if the acceptable range of voltage at some node in an analog circuit is $[V_{nom} - V_{tol}, V_{nom} + V_{tol}]$, then the faulty behavior can take a whole spectrum of values outside this nominal range. One possible fault model for this situation could be to have a resistor tied to the supply rail and changing the value of that resistor to emulate the incorrect spectrum of voltage values. Unfortunately, there is no one resistance value (or fault-size) that can change the voltage at the node to all incorrect values in the spectrum.

A number of resistor values have to be used to sample the faulty voltage spectra sufficiently. So a large number of fault-injections may be necessary to model a fault even at a single node of an analog circuit. This complexity of fault models makes the model-based testing of analog circuits an unsuitable proposition. The prevalent practice in the industry is to use a large set of signals to functionally qualify or test the circuit. Applying these test

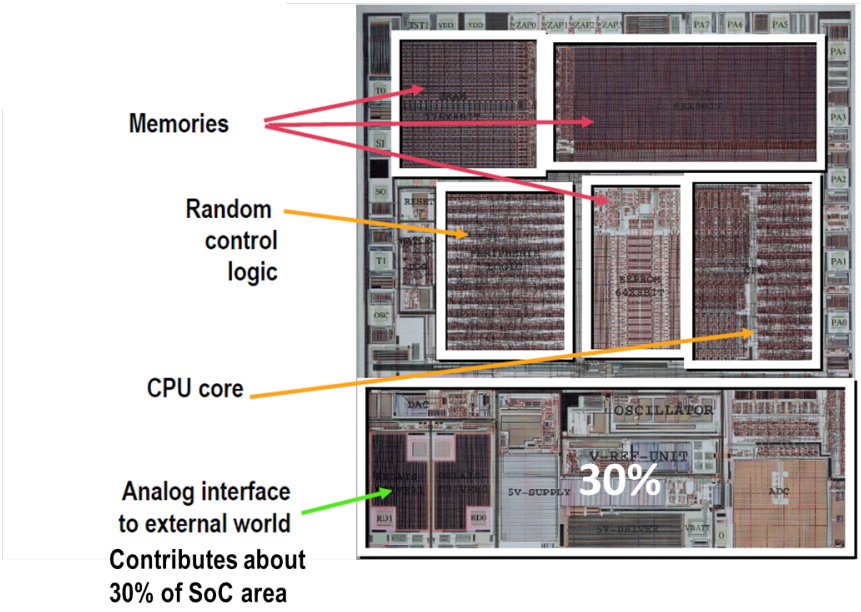


Figure 1.3: Mixed-signal System-on-Chip (SoC) showing size of analog block as a fraction of total die area. Analog interface contributes to about 30% of the total die area. Chip micrograph courtesy of Neolinear [107].

signals to test analog circuits can take disproportionately large amounts of time. An often-quoted number is that analog test take as much as 50% of the total test-time in spite of the analog circuitry occupying less than 15% of the die-area [2]. See for example the micrographs of two mixed-signal system-on-chip (SoC) integrated circuits shown in Figures 1.3 and 1.4. Both have fairly complex analog features, yet the analog circuit size is no greater than 30%.

1.4 Important Challenges in RF/Analog/Mixed-signal Circuit Testing

Previous sections show that analog circuits find their way on almost every system-on-chip type of integrated circuit besides dedicated custom-analog circuits. Heterogeneous integration, increasing wafer sizes, and very fine device geometry have contributed to an increase in analog circuit failure modes that can be harder to catch, degrade the circuit specification in ever more subtle ways, and impact revenue with higher defect level and consequent customer returns. Added to that, innovations in test technology have not kept up with the decreasing manufacturing cost per transistor. As can be seen in the plot in

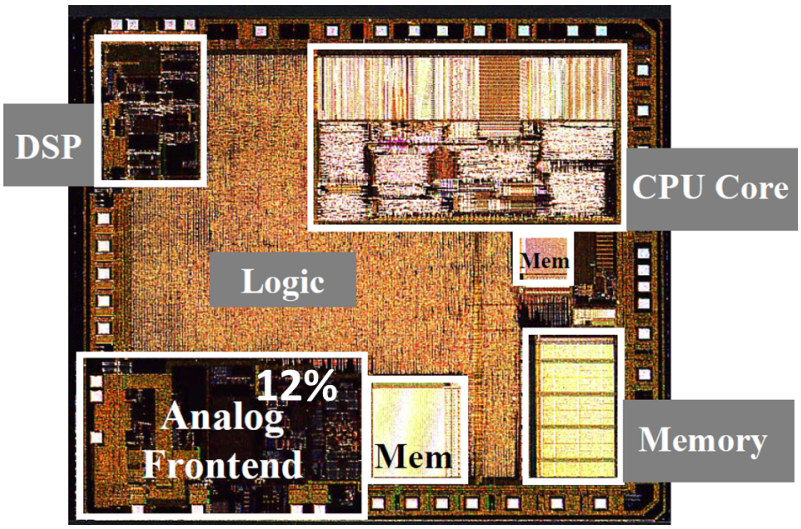


Figure 1.4: Mixed-signal System-on-Chip (SoC) showing size of analog block as a fraction of total die area. Analog interface contributes to about 12% of the total die area. Chip micrograph courtesy of Frank Op't Eynde, Alcatel [107].

Figure 1.5, test cost has remained fairly constant with the passing of years, while the cost of manufacturing a transistor has dropped steadily [1]. Furthermore, though analog circuits contribute less than 10-20% of the chip area, they account for over 50% of the test cost [2]. This can also be noticed in from the plot in Figure 1.5 where the analog test cost per transistor is almost an order of magnitude higher than digital test cost per transistor.

Test cost stemming from long test-times on expensive ATE is the underlying theme of important test problems in analog/mixed signal circuits.

1. Non-linear, continuous-time, continuous-amplitude nature of analog circuits:

   Most analog circuits are non-linear, continuous-time, and continuous amplitude in nature and that makes it a computational challenge to both implement automatic test generation algorithms, and store the large amounts of waveform data that is to be applied to the circuit-under-test in a production test environment.

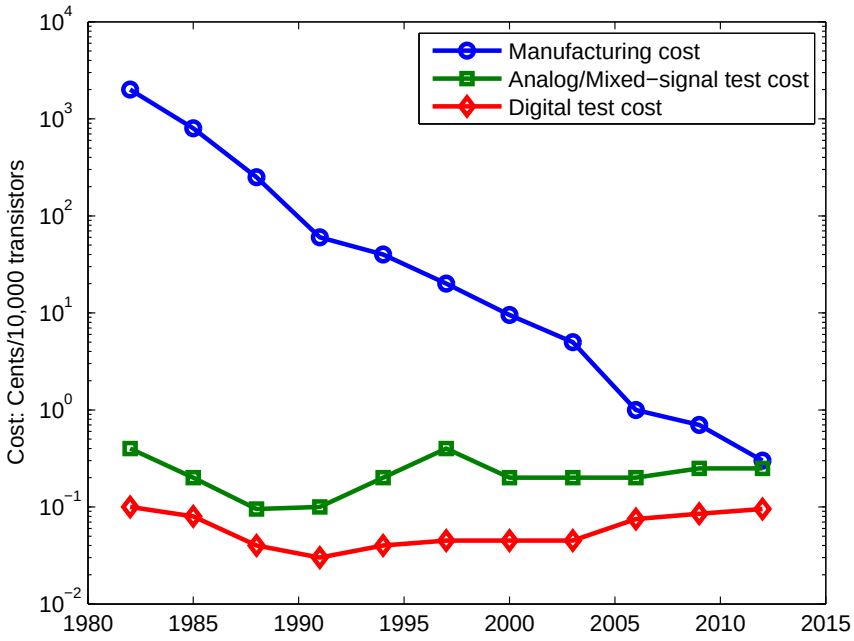


Figure 1.5: Manufacturing cost per transistor on a die has steadily decreased, while test cost per transistor has remained almost constant [1, 2]. Around 2014, it is expected that testing a transistor will cost more than manufacturing one. Also of note is that the analog/mixed-signal test cost per transistor is almost 10 times that of the digital test cost per transistor.

2. "Functionally-good-enough" testing does not cut the deal:

   Testing if a circuit is good-enough (or functional) for some specifications can be relatively easy, but extracting the absolute value of that specification can involve significantly higher effort. For example, in specification testing an RF transceiver, the circuit can be qualified as good if it passes a simple loop-back test. In a loop-back test, the transmitter is tied back to the receiver and the transceiver is considered "pass," if it meets all the receiver specifications, but to make sure that its specifications meet all the regulatory compliance requirements and binning it within a performance bin can be more difficult. Further not all wireless standards permit concurrent operation of transmit and receive modes in a transceiver (which is a prerequisite for loop-back test), and designing the circuit enable this capability can involve major design effort and consequent cost.

3. Inadequate signal visibility at the circuit output:

   Analog circuits for specific functions can be small and deeply embedded within a larger circuit. Bringing out these signals to the pads without degrading the signal quality can be a challenge. Further the measurement inaccuracies due to noise (and consequent lack of repeatability) may call for longer measurement times to average out any noise induced errors. Such measurement errors due to noise is uncommon in digital circuits due to the inherent noise margins.

4. Process variation has made life difficult not only for designers, but also for test engineers:

   Random manufacturing process variation can have significant impact on analog performance parameters. This is because analog circuits are designed with stringent matching requirements (for example, transistors in both the legs of a current-mirror circuit [50, 51] should be a replica of each other lest we risk a high offset current in one branch and the resulting non-linearity if the circuit were to be used in an amplifier). Traditionally testing for sizable manufacturing defects has been the primary concern during test. With process variation induced local variation of circuit parameters, distinguishing between random process variations and recurring small manufacturing defects can be difficult if the deviation in nominal functional performance and defective circuits is small. This is an important concern in analog circuits much like the problem encountered in distinguishing small-delay faults from process variation induced delay faults in digital circuits.

In the next section, we review the efforts spent on RF/Analog circuit testing and diagnosis since the early second-half of the twentieth century.

1.5 A Brief History of RF/Analog Test and Diagnosis

Majority of the circuits before the 1960s were analog. These circuits were usually made with discrete components on printed-circuit-boards. There were minimal, if any, monolithic integrated circuits. The traditional research focus was not as much on testing these circuit boards as it was on diagnosis of faulty components on the circuit board. The challenge traditionally lay in determining which component was at fault, so that the broken circuit could be fixed by replacing the faulty component causing the faulty output. This was so because integrated circuits were still nascent, and it was expensive to discard the entire circuit board instead of replacing the few faulty components. The premise was that if there are any circuits that are bad, it is probable that the faulty components could be identified based on certain uniquely associable attributes of the outputs to the components in the circuit. Many researchers [17, 19, 46, 62, 64, 73, 87, 144, 150] proposed several unique and interesting solutions to the diagnosis problem, which is essentially a fault localization problem. In addition, researchers have also worked on the fault-prediction problem [11, 108, 109, 149], where the circuit output is continuously monitored to predict if any of the circuit-components are about to fail, so they can be replaced in advance of an actual failure. Clearly fault-prediction is a more challenging problem than fault-diagnosis. We will first examine the different fault-diagnosis techniques that have been proposed in literature.

1.5.1 Taxonomy of Analog Circuit Fault-Diagnosis Techniques

Several different criteria could be used for categorizing fault-diagnosis techniques. The popular method of classification is based on the stage in the testing at which simulation of the circuit is undertaken [97, 106, 110]:

- Simulation-before-test, and
- Simulation-after-test.

Figure 1.6 [17] shows a taxonomy of fault-diagnosis techniques based on the above criteria.

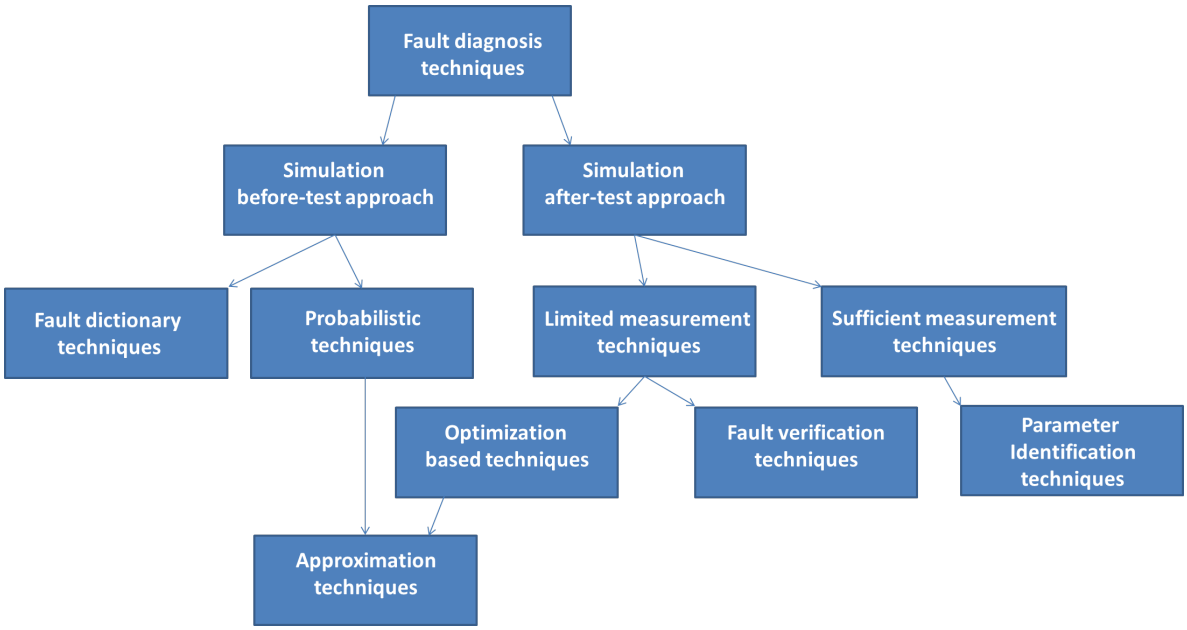


Figure 1.6: A possible classification of analog circuit fault-diagnosis techniques [17].

Fault Dictionary Based Diagnosis

Fault-dictionary techniques classified under simulation-before-test techniques in Figure 1.6 are similar to the widely used fault-dictionary based diagnosis approaches for digital circuits [7, 33]. The first step is to define the most likely faults that can be expected in a given circuit. Defining faults is an important step as the dictionary-size is limited by number of faults defined. An appropriate number of test responses are then captured by simulating the circuit-under-test (CUT) by injecting the defined faults one-by-one, such that unique identification of each fault can be possible by deductive reasoning based on the captured responses for all the applied tests before actually subjecting the circuit in question to test. At the time of test, the captured responses are used to identify the fault or localize it to a small 'ambiguity-set' of faults. The test responses can be captured in frequency domain [31, 88, 89, 133, 148] or in the time domain [113, 132, 147], or as a combination of both [78, 114].

Diagnosis Based on Parameter Identification Techniques

Parameter identification techniques, grouped under simulation-after-test approach in Figure 1.6 involves estimating the deviation in nominal values of circuit components based on voltage/current measurements made at specific nodes in the circuit-under-test for a known input response. The nominal component values and topology of circuit-under-test is known a priori. The deviations in the component values from their nominal values is uniquely determined by solving the set of linear or non-linear equations of the circuit (as determined by the circuit topology). Such circuits for which component values are uniquely determinable based on a few measurements are said to be element-value-solvable [20, 21, 22] circuits and are amenable to parameter identification techniques.

Diagnosis Based on Fault Verification Techniques

Fault verification techniques are based on the premise that for a circuit of n_c components, with n_m measurements taken at test, all the faulty elements (n_f in number) can be uniquely identifiable if n_f is very small, such that the inequality $n_f << n_m < n_c$ is satisfied. The faulty elements are identified by checking the consistency of certain equations which are invariant on the changes in the faulty component values [49, 69, 105, 146].

Approximation Techniques for Diagnosis

Approximation techniques are able to localize faults with limited number of measurements. Two prominent types of approximation techniques are probabilistic [30, 71] and optimization-based [60, 81, 102]. In *probabilistic diagnosis techniques* all the circuit fault-simulation is done before test and can be classified under simulation-before-test. Their working principles are very similar to the dictionary based approach. *Optimization techniques*, on the other hand, optimize some pre-determined criterion to find the most likely faulty element. For example, the L_2 approximation technique [81, 102] uses weighted least squares

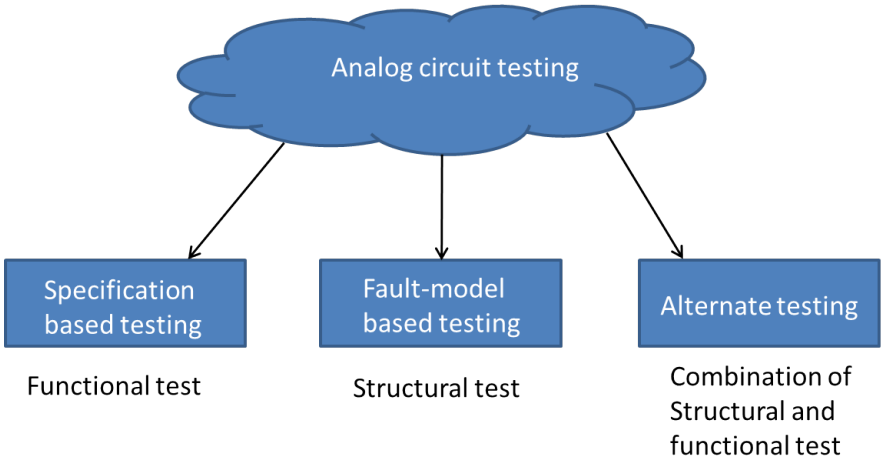


Figure 1.7: A possible classification of analog circuit test techniques.

criterion in identifying the–most-likely faulty element–the element that has undergone the largest deviation from its nominal value.

However, with the advent of integrated circuits, things began to change. Cost of manufacturing even complex circuits, with fairly large component counts, was cheaper than building the bulky boards. The focus slowly shifted from finding the faulty component, or diagnosis, to finding out if the overall circuit behaved as it was designed to behave. We will now examine taxonomy of efforts in analog circuit testing that are geared towards different aspects of the test problem, all of which can be either categorized as aiming to reduce the analog test cost, or increase the testability of the circuit and test-quality.

1.5.2 Taxonomy of RF/Analog Circuit Test Techniques

Figure 1.7 shows the taxonomy of test techniques for analog/RF circuits. The different analog test techniques that are proposed in literature can be classified under three broad categories: functional, structural, and alternate (combination of functional and structural) testing. We shall now review each of the categories and sampling of different test techniques that have been proposed under each of those categories.

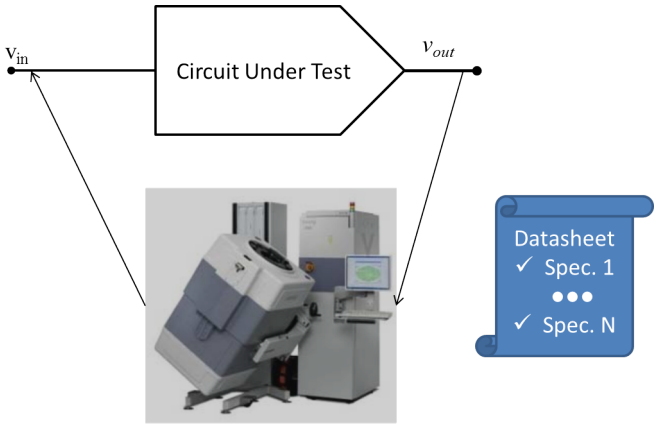


Figure 1.8: Specification testing of analog/mixed-signal circuits in a production test setting.

Specification-Based Testing

The traditional and widely prevalent approach to analog/RF test has been to test the circuit specifications against a list of acceptable limits for each of those specifications. The circuit is deemed to be "Pass," if all its specifications are within the acceptable limits; else it is considered "Fail". Figure 1.8 shows an illustrative picture of how specification based testing is carried out in a production test setting. This approach, though widely prevalent, is expensive even for a pass/fail type of test. The higher test cost stems from large amounts of input stimulus to be applied on the circuit-under-test for measuring all the specifications contributing to the test time on expensive test equipment [32, 79, 91, 112]. In addition, there is the simulation overhead to develop the input stimulus needed for production testing of all specifications [66, 82, 153].

Fault-Model Based Test Techniques

In fault-model based test techniques, the primary objective is to abstract the many physical defects that occur in manufacturing into its electrical equivalent such that tests can target these faults instead of the circuit specifications. The expectation is that testing for these faults will sufficiently cover all the specifications and will do so in a shorter time than the time required for testing the specifications themselves. Typical fault models for

analog circuits are component opens and shorts that mimic large defects that can significantly deviate the behavior of the component. Such faults are known as *catastrophic faults*. Examples of catastrophic faults can be resistor open or short. Defects that lead to small deviations in functionality of the circuit components are modeled as fractional drifts from the nominal values of the circuit element (usually beyond the component tolerance limit), and are called *parametric faults or soft faults*. Examples of parametric faults can be $\pm 10\%$ deviation in the nominal value of the resistor. Number of such fault models have been developed for different components in analog circuits [141]. Different fault-model based test schemes [29, 36, 53, 55, 57, 58, 80, 90, 100, 101, 130, 131] have been proposed in literature. We briefly discuss a representative set of these techniques.

Sensitivity based test and diagnosis techniques [57, 58, 129] constitute testing circuit specifications using the sensitivity of the specifications to components in the circuit. The sensitivity, S_p^C, of a circuit-specification, C, to a circuit-component, p, is defined as:

$$S_p^C = \frac{\frac{\delta C}{C}}{\frac{\delta p}{p}} \tag{1.1}$$

This sensitivity of specifications to the circuit components is leveraged to both test and diagnose the circuit for component faults. Whenever a circuit component undergoes deviation from its nominal, fault-free value, multiple circuit specifications can be tracked, and along with the sensitivity matrix relating the specifications to the circuit components, the most likely circuit component at fault can be determined.

Transfer function based testing [53] proposes the use of modeling the circuit in the frequency domain through the transfer function of the circuit's output with respect to its input. By using a frequency rich input signal, the transfer function of the circuit-under-test is estimated. This transfer function is then compared with the ideal circuit transfer function and any deviation in the coefficients of transfer function beyond an acceptable threshold is treated as a "fail," and a full conformance of all coefficients to pre-determined limits on

the coefficient values is treated as a "pass." The acceptable limits on the coefficients are determined by evaluating the coefficients at different fault sizes of the circuit components.

Alternate Test Techniques

Alternate test techniques [56, 151, 156, 154] combine the prowess of fault-model based testing with specification-based testing, in that, they target certain key circuit variables such as currents and voltages (commonly referred to as circuit-signatures) at critical nodes instead of the actual specification, yet they deliver a go/no-go judgment on the circuit-under-test based on whether or not the CUT meets all the specification limits set in the data-sheet. Chapter 2 discusses this approach in detail and we reserve this discussion until then.

1.5.3 Efforts on Test Cost Reduction for Analog Circuits

Test Re-ordering

Test re-ordering involves changing the sequence of specification tests in order to optimize the test sequence for some predetermined objective. Test sequence can be optimized to reveal the failure modes of the devices, which may be helpful early in the production test setting for yield ramp up by identifying the most common causes of failure and fixing them [83, 85]. As the process flow matures, an objective to be optimized for is the test-time since test-time (the time spent by DUT on an expensive ATE) is an important contributor to the overall production test cost [25].

Redundant Test Elimination

Production test cost is primarily due to the long test-times (stemming from the long-input stimuli) needed for RF/analog devices. With specification tests, where different specifications are tested for in sequence, there is a possibility of dropping certain specifications that may subsume other specifications. For example in case of an ADC testing if the integral

non-linearity (INL) specification is ±0.5 LSB and differential non-linearity (DNL) specification is ±1 LSB, then there is no need for a separate code sweep measurement for DNL specification testing. Eliminating tests for such redundant specifications has been proposed in [84]. Similarly, depending on the chip fall out data from the failed chip statistics, one may be able to leverage the tests that uncover the most defects or fail the most chips. Keeping such tests in the test flow helps retain the quality of the shipped parts while cutting out unnecessary tests that do not add value to the test flow. Techniques based on statistical analysis to eliminate redundant tests for analog and mixed-signal circuits have been proposed in [24, 25].

DfT Efforts in the Analog/Mixed-Signal Test Domain

As predicted in the test/manufacturing cost curve shown in Figure 1.5, over the years, the cost of putting a transistor on the die has gone down exponentially and is converging with the cost of testing one. It is predicted that the future cost of circuits will be limited by its test cost. This has led to the explosion of techniques to drive the test cost lower by adding extra hardware on the chip such that the manufacturing cost incurred in the process is offset by the test cost savings. Several researchers have developed design-for-test (DfT) techniques needed to address this problem. The most prominent industry-wide DfT for analog portions in a mixed-signal SoC is the IEEE standard analog bus for test access to analog blocks in a DUT. Literature on DfT other than test access for analog and mixed signal circuits has primarily been on built-in self test schemes for ADC/DAC [14, 145].

1.6 Contributions of this Thesis

The principal problem addressed in this thesis is that of designing high-sensitivity circuit-test signatures that are capable of uncovering both parametric and catastrophic faults in RF/analog/mixed-signal circuits. In addition, the proposed signatures have high correlation with specifications of the circuit so that these circuit-signatures can replace actual

circuit specifications as is the practice in alternate test framework for RF/analog and mixed-signal circuits. Further, these signatures have been demonstrated to work well for diagnosis of faulty circuit elements. Finally, bounds on the defect level and fault coverage achievable while using these signatures is theoretically evaluated and validated through simulations on a number of benchmark RF/analog circuits.

1.7 What Lies Ahead?

Chapter-wise summary of the thesis is as follows. First chapter provided an introduction to the analog test problem, important challenges today in this area, and the existing methods in the literature. In the second chapter, entitled "Signature Based Testing of RF, Analog and Mixed-Signal Circuits," we take a closer look at the use of signatures in lieu of actual specifications. This chapter forms the basis of the remaining chapters in the thesis which builds on the notion of signatures, thereby proposing stronger and better ones as we go try to increase their sensitivity and correlation to specification measurements. In Chapter 3, we introduce polynomial coefficients of the circuit function which are used as signatures in a closed-form sense to build a model that can accurately detect parametric faults (also known as soft faults). Chapter 4 describes an enhanced sensitivity transformation on polynomial coefficients called V-transform that can deliver almost confidence levels of up to 98% in the detected parametric faults. Chapter 5 discusses an alternate signature that needs little or no input signal design effort. It leverages moments of the probability distribution at the output to uncover faults that are otherwise hidden. It uses a simple distribution function of the input. Chapter 6 provides a formulation, with examples to compute upper bound on the defect level and lower bound on the fault coverage achievable in signature-based test methods. We draw conclusions in Chapter 7, with some thoughts forward-looking ideas that can further enhance the correlation of circuit-signatures to specification through adaptive testing.

Chapter 2

Signature Based Testing of RF, Analog and Mixed-Signal Circuits

2.1 The Need for Circuit Signatures

In a conventional specification based test methodology, as we saw in the previous chapter, the circuit is classified as "good"or "bad" depending on whether it conforms to the designed specifications listed on the data-sheet. To make the measurements on these circuits, expensive instrumentation is needed and devices end up spending considerable amounts of time on these expensive instruments. Circuit signatures circumvent this problem by eliminating the need for measuring the circuit specifications themselves. Instead, signature based testing seeks to replace expensive specification measurement with a direct measurement that is low-cost, in that, it either does not need expensive instrumentation or can be measured in a fraction of the time required to make a full-specification measurement on an expensive tester. Examples of circuit signatures include the supply current drawn by the circuit for a pre-determined input [10], the temperature at specific neighborhoods of the circuit [5], output voltage envelope [155, 156], the spectral coefficients of the supply current and voltage, and a combination of one or more of these [18].

2.2 Attributes of an Ideal Signature

Good signatures are required to be able to replace specification measurements. But the buyer of an integrated circuit is interested in the specification of the part being purchased. So an indirect measurement or signature that seeks to replace specification should be a very good replacement of the circuit-specification. This means, the correlation of the circuits chosen signature to the actual specification should be very good. Further, for signatures to

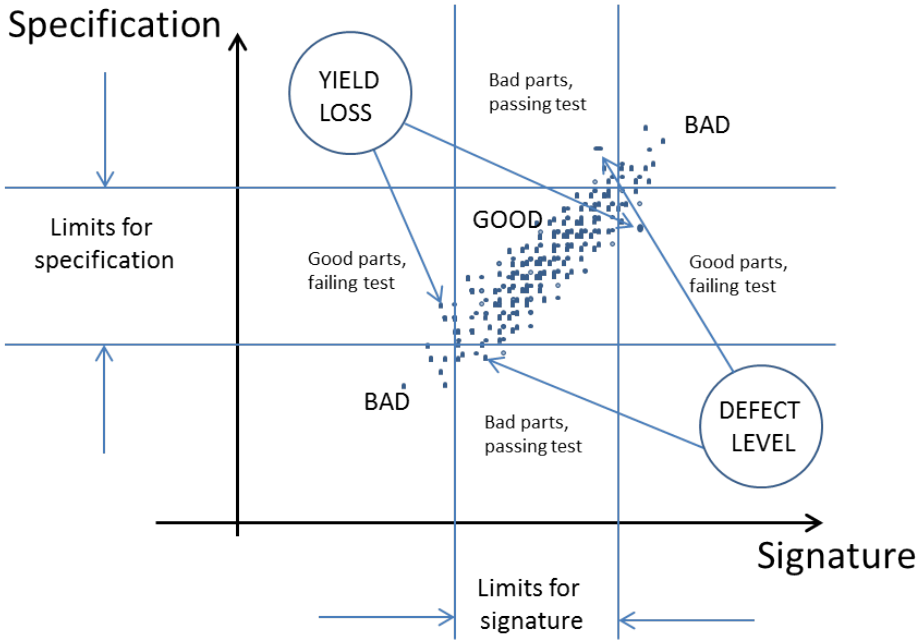


Figure 2.1: Scatter plot of measurements showing the signature on the X-axis and the circuit specification on the Y-axis. An ideal signature will have all points lined up along a straight line such that there is perfect correlation between the signature and the specification.

be practically useful, it should be possible to extract them in a production test setting within a fraction of the time required to extract the actual specification measurements themselves. We now briefly go over each of these attributes:

1. High sensitivity signatures detect sufficiently small parametric faults, thus augmenting existing fault model based test schemes. Signatures should be sensitive to changes in component values beyond their tolerance range. This will ensure they signatures are capable of detecting small parametric faults that are the result of local process variations.

2. High correlation with circuit specifications augmenting alternate circuit test schemes. Signatures are expected to replace actual circuit specifications, so they should be as accurate as possible in predicting the specifications. The more accurate the capability of the signature, the smaller is the yield loss and defect level. Figure 2.1 shows the

scatter plot where the points lined up together (resulting from good correlation between specification and signature) will lead to fewer parts misclassified.

3. Small area overhead requires little additional hardware on chip for production testing.

4. Large number observables handy in diagnosis.

5. Suitable for large class of circuits – there are a variety of classes of analog circuits and the concerned test scheme should be amenable to all of them.

6. Aids distinction of small defects from process variation (PV) induced faults – current need in advanced technology nodes.

7. Amenable to self-test building structures on the circuit, and using signatures that aid in testing the circuits themselves can speed-up the test process as all the fabricated dies can be tested in parallel.

2.3 Analog Circuit Testing Based on Signatures: Test Methodology

1. *Selecting good signatures*

   The choice of test signatures can be a significant factor in the efficacy of the signature test scheme for testing any circuit. A signature that is capable of capturing most specifications over a wide range of values will ensure high test quality, i.e., a test that results in low defect level and yield loss.

2. *Designing good input signals*

   Input signals that bring out all the circuit characteristics are important for ensuring that the signatures serve as a good replacement to the circuit specification. In fact, the combination of input signal and output signature works in tandem to provide the needed robustness for replacing an actual circuit specification with the circuits signature.

3. *Monte-Carlo circuit simulation*

   Circuit components can vary about their nominal values; it is important that the signature chosen have good correlation to the specification over the variation range of the component. Heuristically chosen limits for the component variation is from -3σ to $+3\sigma$. Numbers for σ range from a low of 2% (for thin film resistors) to a high of 15% (advanced technology node transistors) for different components.

4. *Defect filtering*

   This step involves choosing the simulation output by weeding out the outliers to build a good regression model. While it is important the signatures correlate well to the specification over the nominal component range, it is important that there is no correlation between the circuit specification and signature for the outlying component values. Defect filtering is a step that ensures any outliers in the circuit simulation are weeded out so that only the ideal circuit response is available for regression modeling between signature and the circuit specification. Popular defect filters use techniques from machine-learning for distinguishing the circuit-output [137, 139, 140] of a nominally good circuit (whose specification is within some predefined range) from a bad one.

5. *Building a regression model or a neural network classifier*

   Regression modeling is a step where a relational model relating the circuit signatures to the circuit specification that the signature seeks to replace is formulated. Multivariate Adaptive Regression Splines (MARS) [47] is a method that efficiently builds a regression model with only a small number of training samples - essentially pairs of specification and signature for different inputs applied to the circuit in question [59].

6. *Predicting specification from indirect measurements*

   Once an adequate regression model is available, the device-under-test (DUT) is applied with a stimulus to elicit a response, which is then used to predict the specification of

the circuit. If the regression model predicts a specification that is significantly deviant from the nominal range of acceptable specifications, then the DUT is classified as faulty; whereas if the deviation of the predicted specification is close to the boundary of the acceptable specification range, then the DUT can be either retested with actual specification measurements to minimize misclassification or the test procedure can rely solely on the indirect measurement (or signature), in which case there can be a defect level/yield loss penalty.

7. *Improving the models in closed loop*

   The regression model built in the previous step can be continuously tuned to improve the correlation between test signature and specification. This is typically done by having an online training method that updates the regression model based on the actual specification measured on a small sample of training devices right off the production line.

2.4 Conclusion

This chapter introduced the signature based test scheme and described the important constituent steps in this test methodology. In the next chapter we will examine polynomial coefficients as a circuit-test signature. We will demonstrate its use for fault detection and diagnosis on common analog circuits such as elliptic filter and low noise amplifier.

Chapter 3

Polynomial Coefficients as Test Signatures

3.1 Introduction

An analog circuit is called either linear or non-linear based on the type of input-output behavior it displays [38, 68]. Linear circuits preserve linearity and homogeneity of output with the input, and can be described by a linear constant coefficient differential equation [27]. Typically, in the time domain, the output $y(t)$ may be expressed as a function of input $x(t)$, as follows:

$$\sum_{m=1}^{M} a_m \frac{d^m y}{dt^m} + a_0 y = \sum_{n=1}^{N} b_n \frac{d^n x}{dt^n} + b_0 x \qquad (M > N) \tag{3.1}$$

where $a_m, b_n \in \Re \ \forall \ m, n \in \mathrm{Z}$. The general solution for (3.1) is of the form (3.2), where $H(t) \in \Re$ is a real function of time t.

$$y(t) = H(t)x(t) \tag{3.2}$$

Linear circuits are mainly composed of passive components [38]. Typical examples include RC and LC ladder filters and resistive attenuators among others.

In case of non-linear circuits, coefficients $a_m, b_n \ \forall m, \ n$ in (3.1) are functions of x and a general solution in time domain for such circuits can be expressed as in (3.3), where $H_n \ \forall n$ are real functions of t.

$$y(t) = \sum_{n=1}^{n=N} H_n(t)x^n(t) \tag{3.3}$$

Testing of linear circuits is well studied and several methods can be found in the literature [53, 85, 90, 93]. Savir and Guo [53] describe a method in which the circuit is modeled as a linear time-invariant (LTI) system. They obtain the transfer function of the circuit in

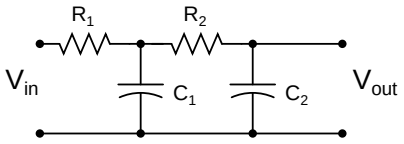


Figure 3.1: A second order low pass filter.

the frequency domain, which is of the following form:

$$H(s) = \frac{\sum_{i=0}^{M} a_i s^i}{\sum_{i=0}^{N} b_i s^i} \qquad (M < N) \tag{3.4}$$

The coefficients of the transfer function, i.e., a_i and b_i, are all functions of circuit parameters and these are tracked to monitor drift in circuit parameters. The CUT is subjected to frequency rich input signals and the output voltage alone is observed. With these input-output pairs they estimate the transfer function coefficients of CUT. Next they compare these transfer function coefficient estimates with the ideal circuit transfer function coefficients, which are known a priori. The CUT is classified faulty if any of the estimated coefficients is beyond the tolerable range. For example, the circuit shown in Figure 3.1 is a second order low pass filter and has a transfer function given below:

$$H(s) = \frac{1}{(R_1 R_2 C_1 C_2)\, s^2 + (R_1 C_1 + (R_1 + R_2) C_2)\, s + 1} \tag{3.5}$$

Clearly the coefficients of the transfer function, $b_0 = 1,\ b_1 = (R_1 C_1 + (R_1 + R_2) C_2)\,,\ b_2 = R_1 R_2 C_1 C_2$, are functions of circuit parameters $R_1,\ R_2,\ C_1,\ C_2$. Assuming single parametric faults, they find the minimum drift in any of the circuit component values that will cause the coefficients b_1 or b_2 (b_0 here is a constant) to drift outside a tolerance range. However, this method [53] *necessarily needs the CUT to be linear*, as a frequency domain transfer function is possible only for a LTI system.

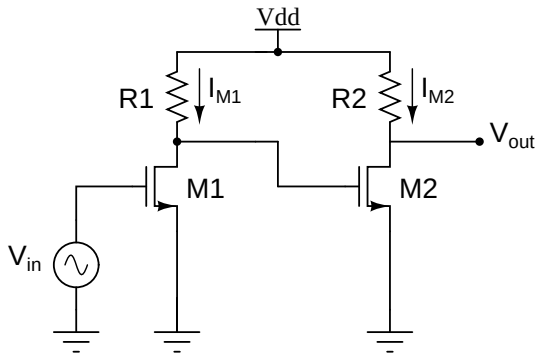


Figure 3.2: Cascade amplifier

Several methods have been proposed for parametric fault testing of non-linear circuits [6, 35, 37, 40, 44, 52, 75, 99]. A prominent method in the industry is the I_{DDQ} testing where quiescent current from the supply rail is monitored and sizable deviations from its expected value are monitored. However, this requires augmentation of the CUT. For example, in the simplest case a regulator supplying power to any sizable circuit has to be augmented with a current sensing resistor and an ADC (for digital output). Subsequently, analysis is performed on the sensed current. I_{DDQ} is found suitable only for catastrophic faults as the current drawn from the supply may be distinguishable when there is some "large enough" fault to change the quiescent current by a distinguishable amount. For example, with resistor R_2 being open in Figure 3.2, the current drawn from supply can change by 50% of its nominal quiescent value. Such faults can typically be found by monitoring I_{DDQ} using a current sensor. However, parametric deviations, say, less than 10% from their nominal value cannot be observed using this scheme. This is especially so for the very deep submicron circuits where the leakage currents can be comparable to the defect induced current [45]. It is therefore useful to develop a method to detect parametric faults while testing with less circuit augmentation.

To address the issue of parametric deviation, we would typically need more observables to have an idea about the parametric drift in circuit parameters. This would mean an increase in the complexity of the sensing circuit. However, we would also want minimal augmentation to tap any of the internal circuit nodes or currents. To overcome these seemingly contrasting

requirements the method intended should have some way of "seeing through" the circuit with only the outputs and inputs at its disposal. References [53, 93] give such strategies for linear circuits as described earlier.

To extend this idea to general non-linear circuits we adopt a strategy where we express the function of the circuit as a polynomial using a Taylor series expansion [72] in terms of input voltage v_{in}, about the point $v_{in} = 0$ as follows:

$$\begin{aligned} v_{out} = f(v_{in}) = f(0) + \tfrac{f'(0)}{1!}v_{in} + \tfrac{f''(0)}{2!}v_{in}^2 + \tfrac{f'''(0)}{3!}v_{in}^3 + \\ \cdots + \tfrac{f^{(n)}(0)}{n!}v_{in}^n + \cdots \end{aligned} \tag{3.6}$$

where $f(x)$ is a real function of x.

This method is very general as any analog circuit can be tested using this model. The technique applies equally well to linear circuits, which are a subclass of the general non-linear circuits considered in this paper. The accuracy, resolution and observability of faults uncovered depends on the degree of expansion of the coefficients in (3.7). Ignoring the higher order terms in (3.6), we can expand v_{out} up to the n^{th} power of v_{in}, which gives us the approximation in (3.7). In order to increase the available observables to better track down parametric faults we can expand v_{out} at multiple frequencies. Thus, we will have $m \times (n+1)$ observables where m is the number of tones (frequencies) including DC at which v_{out} is expanded and n is the degree of expansion [55]:

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + \cdots + a_n v_{in}^n \tag{3.7}$$

where $a_0, a_1, a_2, \ldots, a_n$ are all real functions of circuit parameters $p_k \forall\ k$.

A special case of DC test, that detects a subset of faults, was given in a recent paper [125]. Further, we assume that normal parameter variations (normal drift) in a good circuit are within a fraction α of their nominal value, where $\alpha << 1$. That is, every parameter p_i

is allowed to vary within the range $p_{k,nom}(1-\alpha) < p_k < p_{k,nom}(1+\alpha)\ \forall k$, where $p_{k,nom}$ is the nominal value of parameter p_k. Whenever one or more of the coefficient values slip outside its individual hypercube we get a different set of coefficients reflecting a detectable fault. Therefore, equation (3.8) describes the hypercube for all parameters that correspond to either good machine values or undetectable parametric faults [35, 53, 99]:

$$a_{i,\min} < a_i < a_{i,\max} \quad \forall\ i, \quad 0 \leq i \leq n \tag{3.8}$$

The experimental results and ideas presented in this chapter are taken from the papers [117, 125, 126, 128] by the author. This chapter is organized as follows. Section 2 analyzes the coefficients of the polynomial expansion of the function $f(v_{in})$ and determines the detectable fault sizes of parameters. In Section 3, we describe the problem at hand and discuss the proposed solution with an example. In Section 4, we generalize the solution to an arbitrarily large circuit. Section 5 presents the simulation results for some standard circuits. Section 6 outlines the method of fault diagnosis using the proposed method and we conclude in Section 7.

3.2 Preliminaries

The coefficients $a_i\ \forall i\ 0 \leq i \leq n$ are, in general, non-linear functions of circuit parameters $p_k\ \forall k$. The rationale behind using these coefficients as metrics in classifying CUT as faulty or fault free is based on the dependence of the coefficients on circuit parameters.

3.2.1 Analysis of Polynomial Coefficients

We derive several significant results that are relevant to the subsequent analysis.

Theorem 3.1 *If coefficient a_i is a monotonic function of all parameters, then a_i takes its limiting (maximum and minimum) values when at least one or more of the parameters are at the boundaries of their individual hypercube.*

Lemma 1 *If coefficient a_i is a non-monotonic function of one or more circuit parameters p_i, then a_i can take its limiting values anywhere inside the hypercube enclosing the parameters.*

From Theorem 3.1 and Lemma 1 it is clear that by exhaustively searching the space in the hypercube of each parameter we can get the maximum and minimum values of the polynomial coefficient. Typically this can be formulated as a non-linear optimization problem to find the maximum and minimum values of coefficient with constraints on parameters allowing only a normal drift.

Theorem 3.2 *In polynomial expansion of non-linear analog circuit there exists at least one coefficient that is a monotonic function of all circuit parameters.*

From Lemma 1 and Theorem 3.2 we find that circuit parameter deviations have a bearing on coefficients and monotonically varying coefficients can be used to detect parametric faults of the circuit parameters.

Theorem 3.3 *A continuous non-monotonic function $f : \Re \rightarrow \Re$ can be decomposed into piecewise monotonic functions as follows:*

$$\begin{aligned} f(x) = f(x)u(x_0 - x) + f(x)\left(u(x - x_0) - u(x - x_1)\right) + \\ f(x)\left(u(x - x_1) - u(x - x_2)\right) + \cdots \\ + f(x)\left(u(x - x_{n-1}) - u(x - x_n)\right) \end{aligned} \tag{3.9}$$

where $x_0, x_1, \ \cdots \ x_n$ are all stationary points of $f(x)$ and

$$u(x) = \begin{cases} 1 & \forall\ x \geq 0 \\ 0 & \forall\ x < 0 \end{cases}$$

Using Theorem 3.3, we can express every polynomial coefficient as a monotonic function of circuit parameters and thus we can use every coefficient to track the drifts in circuit parameters.

3.2.2 Definitions

Definition 1 *Minimum size detectable fault (MSDF), (ρ) of a parameter is defined as the minimum fractional deviation of a circuit parameter from its nominal value for it to be detectable with all other parameters being held at their nominal values. The fractional deviation can be positive or negative and is named upside-MSDF (UMSDF) or downside-MSDF (DMSDF), accordingly.*

Definition 2 *Nearly-minimum size detectable fault (NMSDF), (ρ^*) of a parameter is defined as some fractional deviation of the circuit parameter from its nominal value with all the other parameters being held at their nominal values that is close to its MSDF with an error, ϵ (infinitesimally small). That is,*

$$\epsilon = |\rho - \rho*| \qquad\qquad \epsilon << 1 \tag{3.10}$$

NMSDF also has notions of upside and downside as in the case of MSDF. In equation (3.10), ϵ can be perceived as a coefficient of uncertainty about the MSDF of a parameter. Let ψ be the set of all coefficient values spanned by the parameters while varying within their normal drifts, i.e.,

$$\psi = \{\upsilon_0, \upsilon_1, \cdots, \upsilon_n \,|\upsilon_0 \in A_0, \upsilon_1 \in A_1, \cdots, \upsilon_n \in A_n\}$$
$$\forall_k \quad p_{k,nom}(1-\alpha) < p_k < p_{k,nom}(1+\alpha)$$

Note that by Definitions 1 and 2, ψ includes all possible values of coefficients that are not detectable. Any parametric fault inducing coefficient value outside this set ψ will result in a detectable fault.

3.3 Problem Description and Sketch of Solution

We shall first give an illustrative example of calculation of limits for polynomial coefficients for a simple circuit using MOS transistors. We shall follow this up with MSDF values for the circuit parameters.

Example: A two stage amplifier

Consider the cascade amplifier of Figure 3.2. The output voltage V_{out} in terms of input voltage results in a fourth degree polynomial equation as follows:

$$V_{out} = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + a_4 V_{in}^4 \tag{3.11}$$

where the constants a_0, a_1, a_2, a_3 are defined symbolically in (3.12) for M1 and M2 operating in saturation region, as follows

$$a_0 = V_{DD} - R_2 K \left(\frac{W}{L}\right)_{M2} \{(V_{DD} - V_T)^2 + R_1^2 K^2 \left(\frac{W}{L}\right)_{M1}^2 V_T^4 - 2(V_{DD} - V_T) R_1 \left(\frac{W}{L}\right)_{M1} V_T^2\}$$

$$a_1 = R_2 K \left(\frac{W}{L}\right)_{M2} \{4R_1^2 K^2 \left(\frac{W}{L}\right)_{M1}^2 V_T^3 + 2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_{M1} V_T\}$$

$$a_2 = R_2 K \left(\frac{W}{L}\right)_{M2} \{2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_{M1} - 6R_1^2 K^2 \left(\frac{W}{L}\right)_{M1}^2 V_T^2\}$$

$$a_3 = 4V_T K^3 \left(\frac{W}{L}\right)_{M1}^2 \left(\frac{W}{L}\right)_{M2}^2 R_1^2 R_2$$

$$a_4 = -K^3 \left(\frac{W}{L}\right)_{M1}^2 \left(\frac{W}{L}\right)_{M2}^2 R_1^2 R_2 \tag{3.12}$$

Nominal values of $V_{DD} = 1.2\text{V}$, $V_T = 400\text{mV}$, $\left(\frac{W}{L}\right)_{M1} = \frac{1}{2}\left(\frac{W}{L}\right)_{M2} = 20$, and $K = 100\mu A/V^2$ are substituted to get coefficients in terms of parameters R_1 and R_2 as given by,

$$\begin{aligned}
a_0 &= 1.2 - R_2(2.56 \times 10^{-3} + 1.024 \times 10^{-7} R_1^2 - 5.12 \times 10^{-4} R_1 \\
a_1 &= 4.096 \times 10^{-9} R_1^2 R_2 + 5.12 \times 10^{-6} R_1 R_2 \\
a_2 &= 1.28 \times 10^{-5} R_1 R_2 - 1.536 \times 10^{-8} R_1^2 R_2 \\
a_3 &= 2.56 \times 10^{-8} R_1^2 R_2 \\
a_4 &= 1.6 \times 10^{-8} R_1^2 R_2
\end{aligned} \tag{3.13}$$

To find the limiting values of the coefficient a_0 we assume the parameters R_1 and R_2 deviate by fractions x and y from their nominal values, respectively. Maximizing a_0 we have the objective function as given by (3.14), subject to constraints 3.15 through 3.19. Note that here we have set out to find MSDF of R_1. Similar approach can be used to find the MSDF of R_2:

$$1.2 - R_{2,nom}(1+y)\{2.56 \times 10^{-3} + 1.024 \times 10^{-7} R_{1,nom}^2 (1+x)^2 - 5.12 \times 10^{-4} R_{1,nom}(1+x)\} \tag{3.14}$$

$$\begin{aligned}
&4.096 \times 10^{-9} R_{1,nom}^2 (1+x)^2 R_{2,nom} \ (1+y) \\
&+5.12 \times 10^{-6} R_{1,nom}(1+x) R_{2,nom}(1+y) \\
&\quad = 4.096 \times 10^{-9} R_{1,nom}^2 (1+\rho)^2 R_{2,nom} \\
&\quad + 5.12 \times 10^{-6} R_{1,nom}(1+\rho) R_{2,nom}
\end{aligned} \tag{3.15}$$

Table 3.1: MSDF for cascade amplifier of Figure 3.2 with $\alpha = 0.05$.

Circuit parameter	%upside MSDF	%downside MSDF
Resistor R_1	10.3	7.4
Resistor R_2	12.3	8.5

$$\begin{aligned} 1.28 \times 10^{-5} R_{1,nom}(1+x)R_{2,nom}(1+y) \\ -1.536 \times 10^{-8} R_{1,nom}^2(1+x)^2 R_{2,nom}\ (1+y) \\ = 1.28 \times 10^{-5} R_{1,nom}(1+\rho)R_{2,nom} \\ - 1.536 \times 10^{-8} R_{1,nom}^2(1+\rho)^2 R_{2,nom} \end{aligned} \tag{3.16}$$

$$\begin{aligned} 2.56 \times 10^{-8} R_{1,nom}^2(1+x)^2 R_{2,nom}(1+y) \\ = 2.56 \times 10^{-8} R_{1,nom}^2(1+\rho)^2 R_{2,nom} \end{aligned} \tag{3.17}$$

$$\begin{aligned} 1.6 \times 10^{-8} R_{1,nom}^2(1+x)^2 R_{2,nom}(1+y) \\ = 1.6 \times 10^{-8} R_{1,nom}^2(1+\rho)^2 R_{2,nom} \end{aligned} \tag{3.18}$$

$$-\alpha \leq x, y \leq \alpha \tag{3.19}$$

The extreme values for x and y on solving the set of equations 3.15 through 3.19 are obtained as, $x = -\alpha$ and $y = -\alpha$, and this gives us the MSDF value for R_1, as ρ,

$$\rho = (1-\alpha)^{1.5} - 1 \approx 1.5\alpha - 0.375\alpha^2 \tag{3.20}$$

Table 3.1 gives the MSDF for R_1 and R_2 based on above calculation.

3.4 Generalization

In general, the calculation as described above cannot be done for an arbitrarily large circuit. Such circuits are handled by obtaining a nominal numeric polynomial expansion of the fault free circuit. This is done by sweeping the input voltage across all possible values and

noting the corresponding output voltages using any of the standard circuit simulators like SPICE [4, 98]. Now, the output voltage is plotted against the input voltage. A polynomial is fitted to this curve and the coefficients of this polynomial are taken to be the nominal coefficients of the desired polynomial. The circuit is simulated for different drifts in the parameter values at equally spaced points from inside the hypercube enclosing each circuit parameter, spaced at a suitably chosen resolution (ϵ). Polynomial coefficients are obtained for each of these simulations. The maximum and the minimum values of a coefficient in this search are taken as the limiting values on that coefficient. This process of modeling the circuit as a polynomial expansion and obtaining limit values on coefficients is repeated at "key" frequencies of interest. For example, the cut-off frequency in case of a non-linear filter can be a good candidate for such characterization. Once the limit values on all coefficients have been determined the CUT is subjected to full range of input at DC and each of the "key" frequencies. Its response to input sweep is curve fitted to a polynomial of order same as the fault free circuit. If there are any coefficients that lay outside the limit values of corresponding coefficients of the fault free circuit, we can conclude the CUT is faulty. The converse is also true with a high probability that is inversely proportional to coefficient of uncertainty ϵ. Flow chart in Figure 3.3 summarizes the process of numerically finding the polynomial and finding the bounds on coefficients. Flow chart in Figure 3.4 outlines the procedure to test CUT using the described method.

3.5 Experimental Results

Example 1: An Elliptic Filter. We subjected an elliptic filter shown in Figure 3.5 to Polynomial Coefficient based test. The circuit parameter values are as in the benchmark circuit maintained by Stroud et al. [70]. We simulated the circuit at four different frequencies. Two of them were chosen close to its 3dB cut-off frequency (f_c), which is 1000Hz. The estimated polynomial expansions obtained by curve fitting the I/O plots at DC and the frequencies f = 100Hz, 900Hz, 1000Hz and 1100Hz are given in 3.21 through 3.25 and

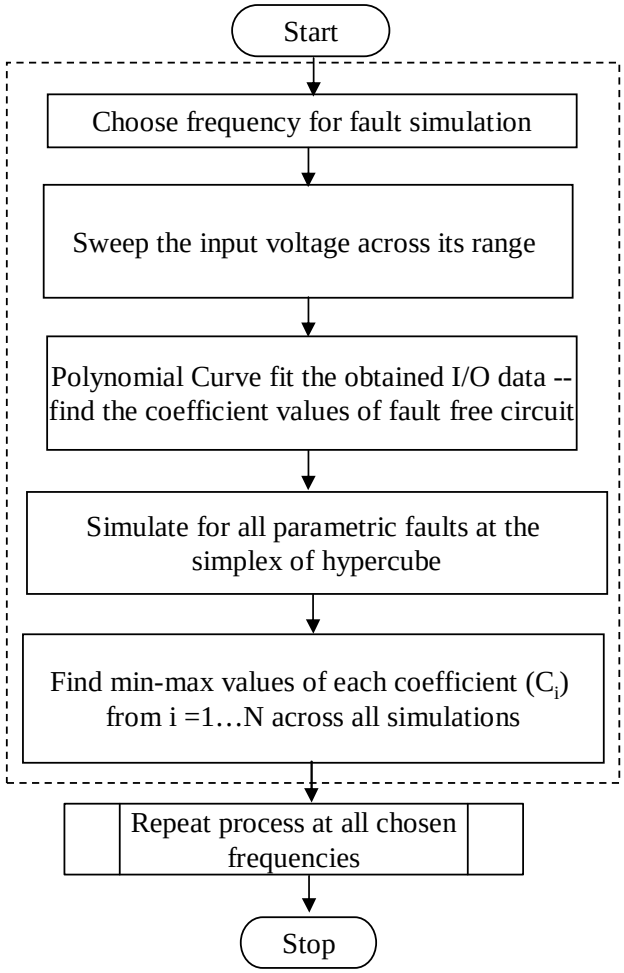


Figure 3.3: Flow chart showing fault simulation process and bounding of coefficients.

the corresponding plots tracing I/O response with polynomial are shown in Figures 3.6 through 3.10. The combinations of parameter values leading to limits on the coefficients for the tone at 1000Hz are shown in Table 3.5. Further, the pass/fail detectabilities of several injected faults are tabulated in Table 3.6.

In our ongoing work, we are testing this technique on other common non-linear circuits like logarithmic amplifiers [63] whose results we will furnish in a forthcoming paper.

$$v_{out} = 4.5341 - 3.498v_{in} - 2.5487v_{in}^2 + 2.1309v_{in}^3 - 0.50514v_{in}^4 + 0.039463v_{in}^5 \tag{3.21}$$

$$v_{out} = 3 + 7.9v_{in} - 11v_{in}^2 + 4.4v_{in}^3 - 0.78v_{in}^4 + 0.049v_{in}^5 \tag{3.22}$$

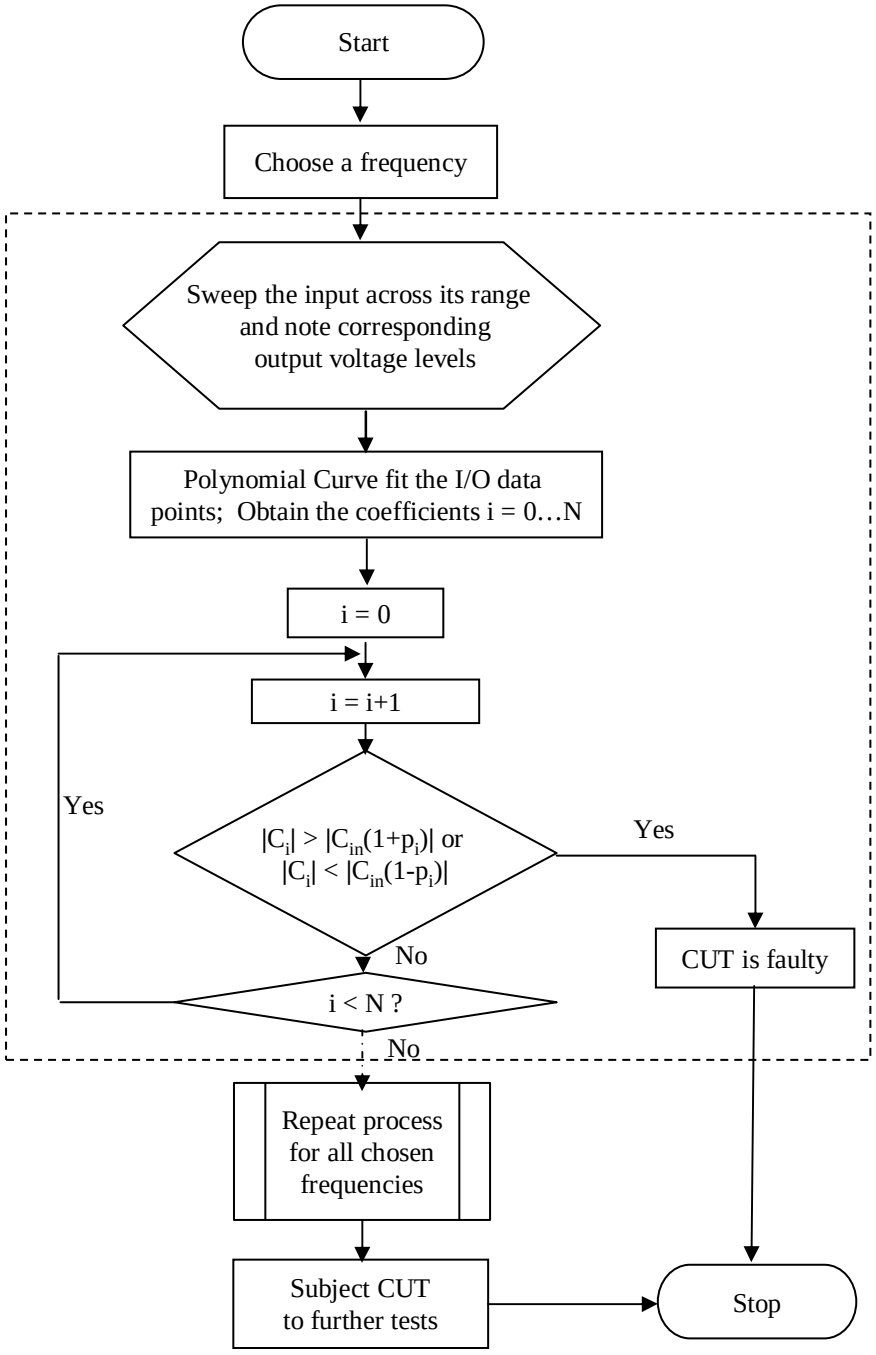


Figure 3.4: Flow chart outlining test procedure for CUT.

$$v_{out} = 2.5 + 5.4v_{in} - 8.6v_{in}^2 + 4v_{in}^3 - 0.77v_{in}^4 + 0.054v_{in}^5 \tag{3.23}$$

$$v_{out} = 1.1707 + 2.4132v_{in} - 3.8777v_{in}^2 + 1.8035v_{in}^3 - 0.3465v_{in}^4 + 0.023962v_{in}^5 \tag{3.24}$$

$$v_{out} = 0.23 + 0.48v_{in} - 0.74v_{in}^2 + 0.34v_{in}^3 - 0.063v_{in}^4 + 0.0043v_{in}^5 \tag{3.25}$$

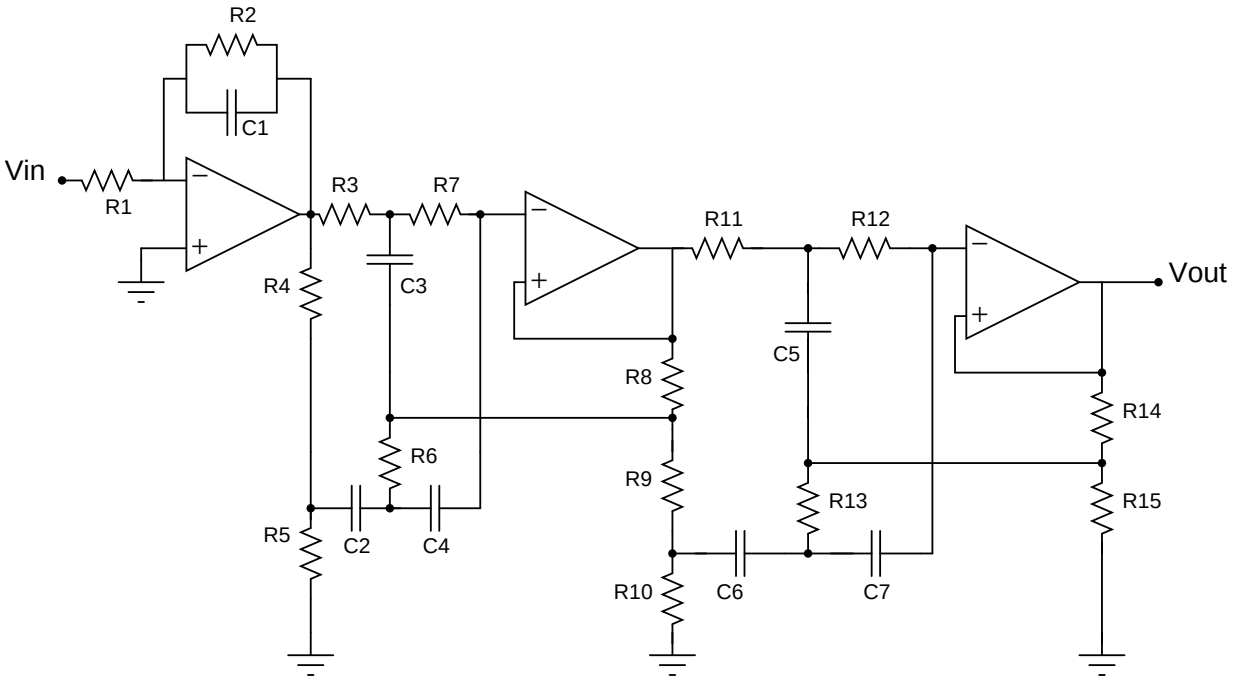


Figure 3.5: Elliptic filter.

Example 2: Low Noise Amplifier (LNA). We simulated a Low noise amplifier shown in Figure 3.12 for polynomial coefficient based test. Notice that the bias current I_{bias} shown in the figure is derived from a current mirror powered by band-gap reference circuitry (not shown). The circuit parameter values were chosen to meet performance specifications tabulated in Table 3.2. We used parametric faults of sizes $\alpha = 5\%$ from their nominal value to find min-max values of coefficients. Figure 3.13 shows the simulated response at four different frequencies, namely, f = 1GHz, 10GHz, 15GHz, and 35GHz and the estimated polynomials obtained by curve fitting a fifth order polynomial are given by equations (3.26) through (3.29), respectively. To obtain these curves, input offset voltage is varied from 0 through 5V as shown (on X-axis), while measuring the output voltage magnitude at each of these input voltage points. As we can see in the figure (on the far right), the output magnitude at 35GHz, drops to about 72% its value at preceding three frequencies, which

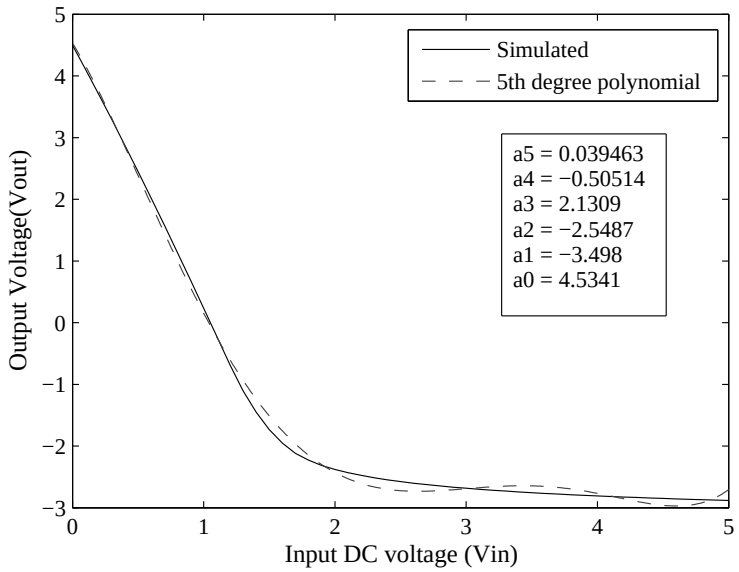


Figure 3.6: DC response of elliptic filter with curve fitting polynomial.

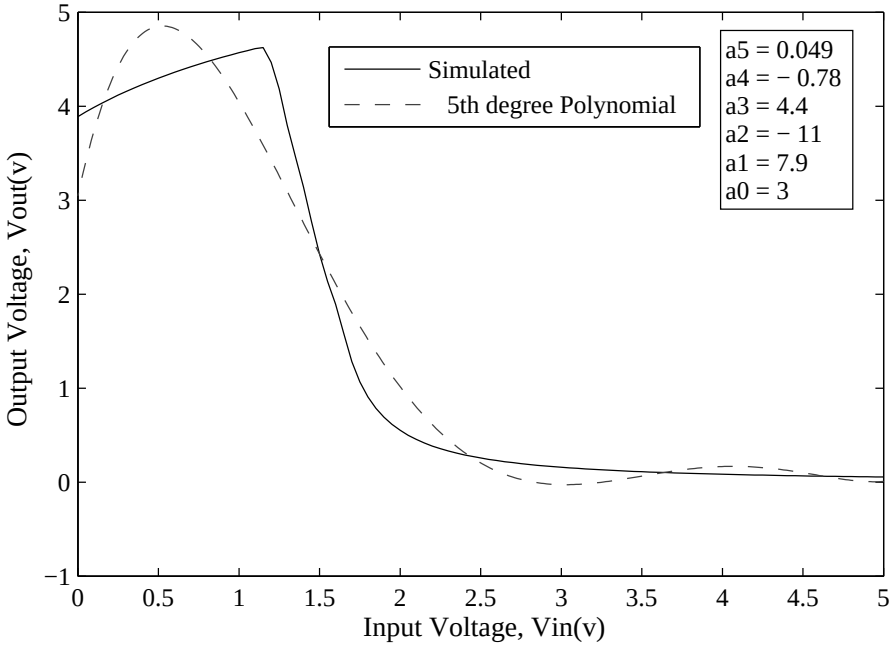


Figure 3.7: Curve-fit polynomial with coefficients at frequency = 100Hz.

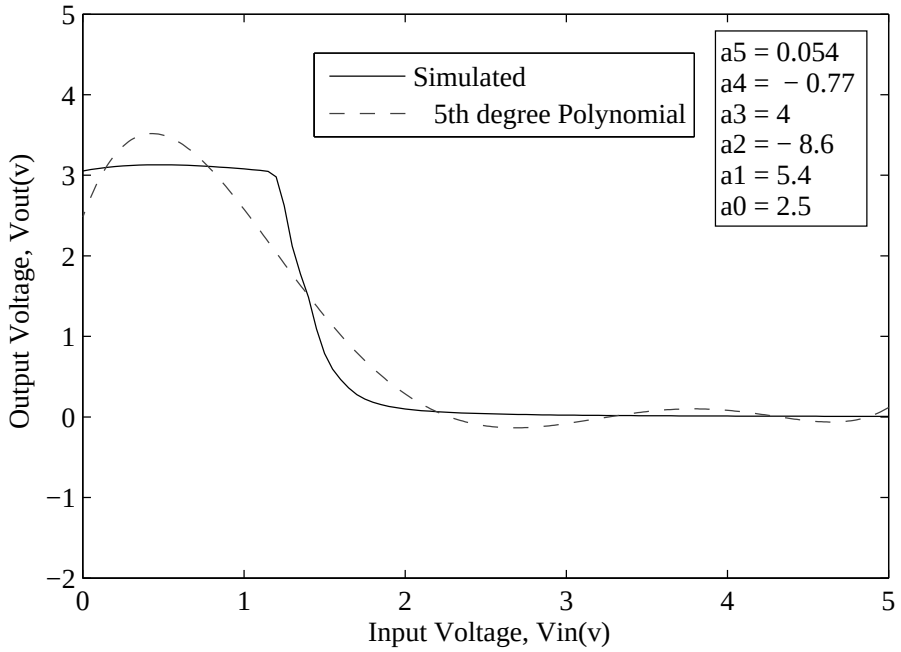


Figure 3.8: Curve-fitting polynomial with coefficients at frequency = 900Hz.

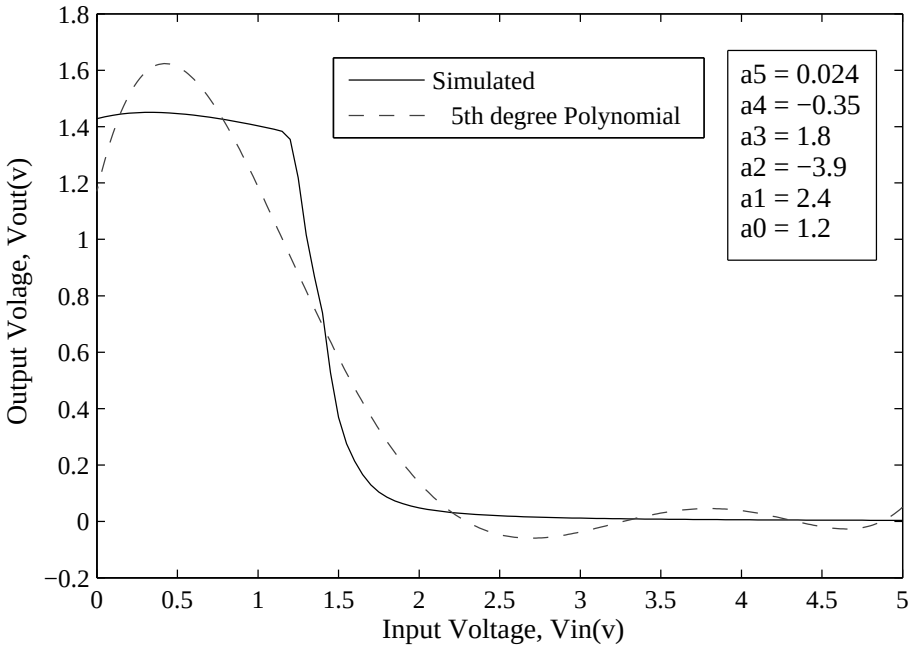


Figure 3.9: Curve-fitting polynomial with coefficients at frequency = 1000Hz.

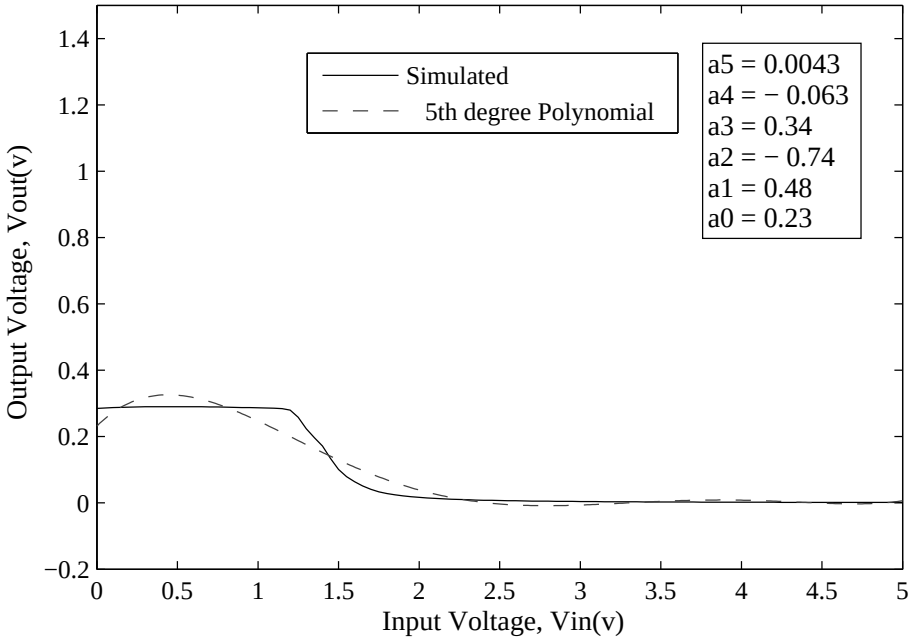


Figure 3.10: Curve-fitting polynomial with coefficients at frequency = 1100Hz.

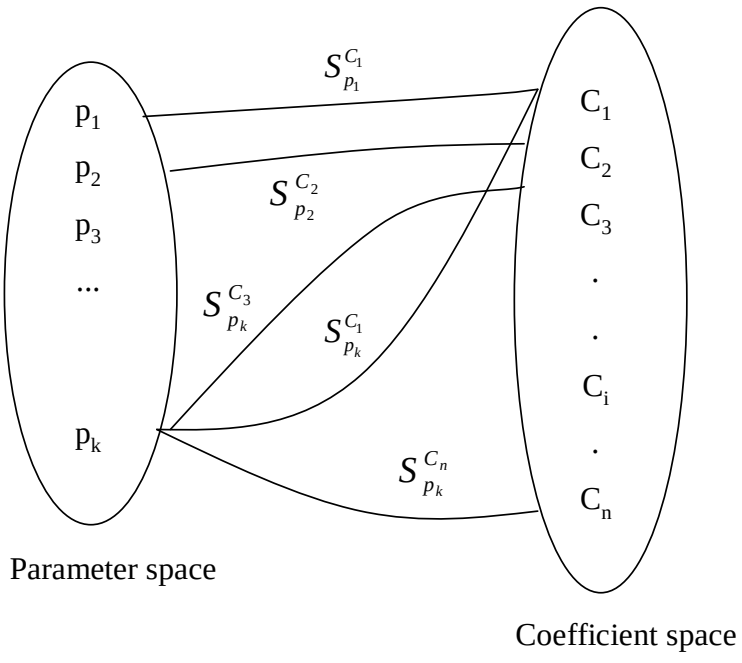


Figure 3.11: Mapping showing one possible relation between various parameters and coefficients.

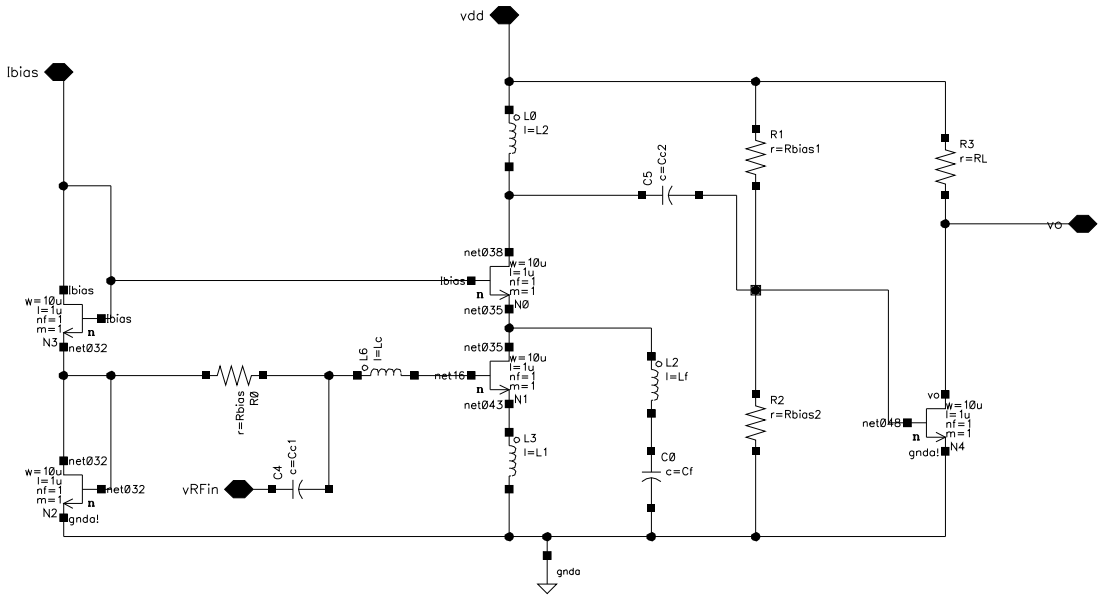


Figure 3.12: Low noise amplifier (LNA) schematic.

Table 3.2: LNA specification.

Performance Parameter	**Nominal Value**
Gain (dB)	16
IIP_3 **(dBm)**	-18
Noise figure (dB)	9.1
S_{11} **(dB)**	-16.5

confirms (in close neighborhood of) 35GHz as the 3dB cut-off, and thereby the ultra-wide bandwidth LNA designed and tested in this example.

Figure 3.14 compares the I/O response of the LNA for three different value of the load resistance R_L.

$$v_{out} = \left(2.5 - 1.498v_{in} - 1.2688v_{in}^2 + 1.139v_{in}^3 - 0.88514v_{in}^4 + 0.039463v_{in}^5\right) \times 10^{-3} \quad (3.26)$$

$$v_{out} = \left(2.36 - 1.348v_{in} - 1.3268v_{in}^2 + 1.049v_{in}^3 - 0.63614v_{in}^4 + 0.04443v_{in}^5\right) \times 10^{-3} \quad (3.27)$$

$$v_{out} = \left(2.12 - 1.267v_{in} - 1.1285v_{in}^2 - 1.016v_{in}^3 + 0.88516v_{in}^4 - 0.052876v_{in}^5\right) \times 10^{-3} \quad (3.28)$$

$$v_{out} = \left(1.95 - 1.068v_{in} + .9268v_{in}^2 + .786v_{in}^3 - 0.77324v_{in}^4 + 0.042v_{in}^5\right) \times 10^{-3} \quad (3.29)$$

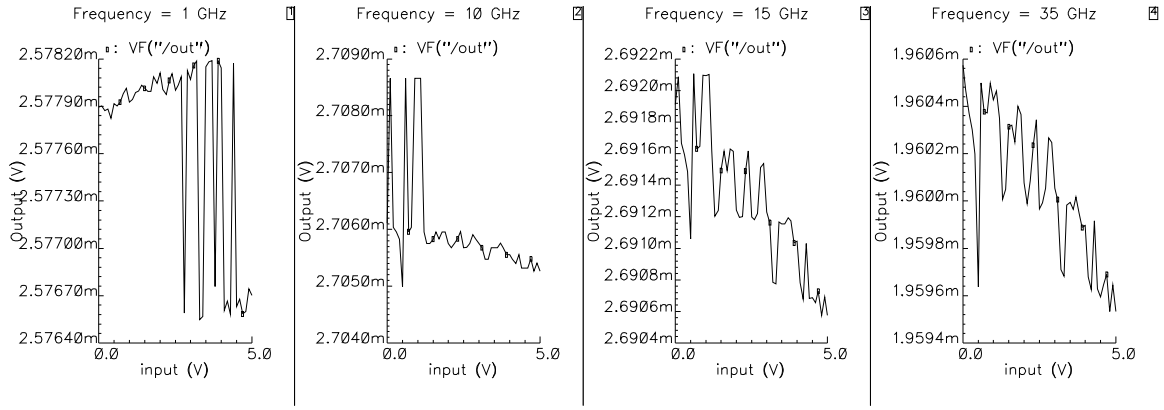


Figure 3.13: I/O response of LNA at four frequencies.

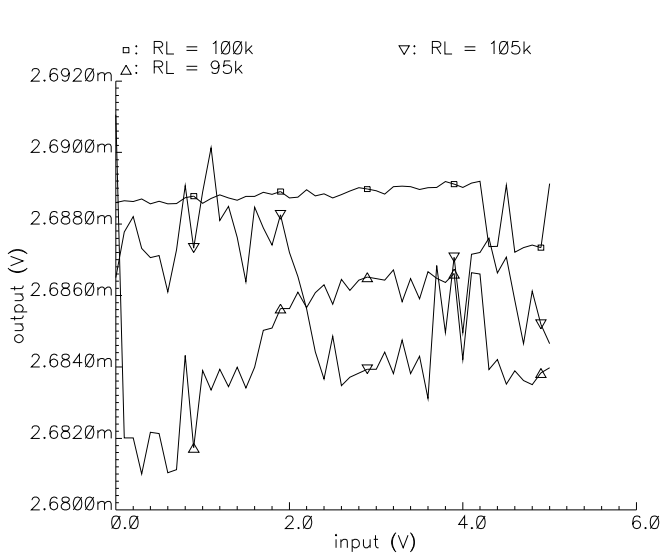


Figure 3.14: Comparison of I/O plots of LNA at 3 different values of load resistance R_L = 95kΩ, 100kΩ (nominal), and 105kΩ.

The combinations of parameter values leading to limits on the coefficients are as shown in Tables 3.3 and 3.4. Some of the circuit parameters are not shown in the table because they do not appear in any of the coefficients and are kept at their nominal values. Further, results on pass/fail detectability of few injected faults are tabulated in Table 3.8. Last column in

Table 3.3: Parameter combinations leading to maximum values of coefficients with $\alpha = 0.05$ for the LNA.

Component (ohm, nH, fF)	a_0	a_1	a_2	a_3	a_4	a_5
$R_{bias} = 10$	10	10	10.5	10.5	9.5	10.5
$L_C = 1$	1	0.95	1.05	0.95	1.05	1
$C_{C1} = 100$	95	95	95	95	95	105
$L_1 = 1.5$	1.425	1.5	1.5	1.425	1.575	1.425
$L_2 = 1.5$	1.5	1.425	1.425	1.575	1.5	1.5
$L_f = 1$	1.05	1.05	1.05	1	1.05	1
$C_f = 100$	105	95	95	105	95	95
$C_{C2} = 100$	95	100	105	95	95	95
$R_{bias1} = 100k$	105k	105k	100k	105k	105k	95k
$R_{bias2} = 100k$	105k	95k	100k	95k	95k	95k
$R_L = 100k$	100k	95k	95k	100k	105k	100k

Table 3.8 shows the diagnosed results of a few injected faults using sensitivity of polynomial coefficients to circuit parameters as described in Section 3.6.

3.6 Fault Diagnosis

Fault diagnosis using sensitivity of output to circuit parameters has been investigated in the literature [129]. We have extended that approach exploiting the sensitivity of polynomial coefficients to circuit parameters. The advantage of the new approach is an improved fault diagnosis without circuit augmentation. Sensitivity of i^{th} coefficient C_i to k^{th} parameter p_k is represented by $S_{p_k}^{C_i}$ and is given by:

$$S_{Pk}^{Ci} = \frac{p_k}{C_i}\frac{\partial C_i}{\partial p_k} \tag{3.30}$$

Table 3.4: Parameter combinations leading to Min values of coefficients with $\alpha = 0.05$ for the LNA.

Component (ohm, nH, fF)	a_0	a_1	a_2	a_3	a_4	a_5
$R_{bias} = 10$	10	9.5	9.5	10	10	10
$L_C = 1$	1.05	0.95	0.95	1	1	0.95
$C_{C1} = 100$	100	105	95	100	95	105
$L_1 = 1.5$	1.425	1.5	1.575	1.575	1.575	1.575
$L_2 = 1.5$	1.5	1.575	1.5	1.425	1.425	1.5
$L_f = 1$	1.05	1.05	0.95	0.95	1	0.95
$C_f = 100$	105	95	95	105	105	105
$C_{C2} = 100$	95	105	100	105	95	105
$R_{bias1} = 100k$	100k	95k	105k	105k	95k	100k
$R_{bias2} = 100k$	100k	105k	95k	95k	105k	95k
$R_L = 100k$	95k	100k	95k	100k	105k	95k

3.6.1 Computation of Sensitivities

Numerical computation of sensitivities given by (3.30) is accomplished by introducing fractional drifts ($=\alpha$) in each component ($p_k \ \forall k$); simulating the circuit and measuring the fractional drift in each coefficient of the polynomial resulting from curve fitting operation. This way the numerical sensitivities are computed and a dictionary is maintained for sensitivities. The complexity in computation of sensitivities is linear in the number N of circuit parameters, i.e., $O(N)$.

3.6.2 Diagnosing Parametric Faults

Restricting ourselves to single parametric faults, we find the descending order of sensitivities of coefficients (with respect to circuit parameter) that have exceeded their limiting values. The parameter with highest sensitivity is said to be at fault with a probability $P(\delta p_k|\delta C_i)$ (which can be interpreted as the confidence in diagnosing fault), given by (3.31), where δp_k is the suspected drift in parameter p_k and δC_i is the measured drift in coefficient.

$$P(\delta p_k|\delta C_i) = \frac{S_{P_k}^{C_i}\delta p_k}{\delta C_i} \tag{3.31}$$

3.6.3 Deducing Faults

At each frequency, the above process of diagnosis is repeated. This gives the set of fault sites above a certain confidence level at each of these frequencies. The intersection of sets of fault sites at all the frequencies (and at DC) gives a fault site with much higher confidence level. That is, if the confidence of diagnosis of a fault site at one frequency is say P_i, then the resulting confidence level after diagnosis at all the frequencies is as follows[94]:

$$P = 1 - \prod_{i=1}^{i=N} (1 - P_i) \tag{3.32}$$

where N is the number of frequencies (including DC) at which the circuit is diagnosed.
The single parametric faults for the elliptic filter in Figure 3.5 were diagnosable with confidence levels up to 60% at each frequency. The resulting confidence level after fault deduction from the four frequencies at which it was diagnosed is about 98.9%. The diagnosis results are tabulated in Table 3.7 for several injected single parametric faults. Another observation worthy of mention here is that the cardinality of set of fault sites detected at frequencies close to cut-off frequency is greater than that at frequencies closer to DC. This can be attributed to higher sensitivity of coefficients to circuit parameters at these frequencies. As a result, fault coverage is better by observing coefficient drifts at frequencies close to f_c. However these frequencies tend to be unfavourable for diagnosis as more than one parameter is likely to have displaced the coefficients out of their respective hypercubes. We can overcome this by looking at the set of fault sites obtained at much lower frequencies than f_c (here DC and 100Hz).

3.7 Conclusion

A new approach for testing non-linear circuits based on polynomial expansion of the circuit function was proposed in this chapter. By expanding polynomial coefficients at critical frequencies the fault coverage of test for parametric (and catastrophic) faults is significantly

Table 3.5: Parameter combinations leading to Max and Min Values of coefficients with $\alpha = 0.05$ at 1000Hz for the elliptic filter.

Circuit Parameters (Resistance in Ω,Capacitance in Farad)												
Nominal Values	Maximum values						Minimum values					
	a_0	a_1	a_2	a_3	a_4	a_5	a_0	a_1	a_2	a_3	a_4	a_5
$R_1 = 19.6k$	18.6k	18.6k	20.5k	20.5k	20.5k	18.6k	18.6k	18.6k	18.6k	18.6k	20.5k	20.5k
$R_2 = 196k$	205k	205k	205k	205k	186k	186k	205k	186k	186k	205k	205k	205k
$R_3 = 147k$	139k	139k	154k	139k	139k	139k	139k	139k	154k	139k	139k	139k
$R_4 = 1k$	950	950	1.05k	1.05k	1.05k	1.05k	1.05k	950	1.05k	950	950	1.05k
$R_5 = 71.5$	75	67	75	67	67	75	75	75	67	67	75	67
$R_6 = 37.4k$	35k	39k	39k	35k	35k	39k	39k	39k	35k	35k	35k	35k
$R_7 = 154k$	146k	146k	161k	161k	146k	146k	146k	146k	161k	161k	146k	146k
$R_8 = 260$	247	273	273	247	247	273	273	247	273	247	273	247
$R_9 = 740$	703	777	703	703	777	703	703	703	777	703	703	703
$R_{10} = 500$	475	525	525	475	525	525	475	525	475	475	525	475
$R_{11} = 110k$	115k	115k	115k	104k	104k	104k	115k	115k	104k	115k	104k	104k
$R_{12} = 110k$	104k	104k	115k	115k	115k	115k	115k	115k	104k	104k	115k	104k
$R_{13} = 27.4k$	28.7k	26k	26k	26k	28.7k	28.7k	26k	26k	28.7k	26k	28.7k	26k
$R_{14} = 40$	42	38	42	38	38	42	42	38	42	42	38	42
$R_{15} = 960$	912	912	912	912	912	1k	1k	1k	912	1k	912	912
$C_1 = 2.67n$	2.5n	2.5n	2.5n	2.5n	2.5n	2.5n	2.8n	2.5n	2.8n	2.8n	2.8n	2.5n
$C_2 = 2.67n$	2.5n	2.8n	2.8n	2.5n	2.8n	2.8n	2.8n	2.8n	2.5n	2.8n	2.5n	2.8n
$C_3 = 2.67n$	2.8n	2.8n	2.8n	2.5n	2.8n	2.8n	2.8n	2.8n	2.8n	2.5n	2.8n	2.8n
$C_4 = 2.67n$	2.5n	2.8n	2.5n	2.5n	2.5n	2.5n	2.5n	2.5n	2.8n	2.5n	2.5n	2.8n
$C_5 = 2.67n$	2.5n	2.5n	2.5n	2.5n	2.5n	2.8n	2.8n	2.8n	2.8n	2.8n	2.8n	2.8n
$C_6 = 2.67n$	2.5n	2.8n	2.5n	2.8n	2.5n	2.8n	2.5n	2.5n	2.8n	2.8n	2.8n	2.5n
$C_7 = 2.67n$	2.5n	2.8n	2.8n	2.8n	2.8n	2.5n	2.8n	2.5n	2.5n	2.5n	2.5n	2.8n

improved, yielding a minimum size of detectable faults in some circuit components as low as 5%. The method has been extended to sensitivity based fault diagnosis with probabilistic confidence levels in parameter drifts. Further the expansion at multiple tones leads to a higher confidence level (up to 98.9%) in diagnosing single parametric fault sites. In the next chapter, we shall discuss the use of V-transform for further enhancing the fault detection capabilities of the polynomial coefficients.

Table 3.6: Results of some injected faults at different frequencies for the elliptic filter.

Injected fault	Coefficients out of Bounds at					Detected
	DC	f_1=100Hz	f_2=900Hz	f_3=1000Hz	f_4=1100Hz	
R_1 down 15%	$a_0 - a_4$	$a_1 - a_4$	a_3, a_5	a_2, a_4	a_1, a_2	Yes
R_2 down 5%	a_2, a_5	a_1, a_3	a_1, a_5	a_1, a_2, a_5	a_1, a_2	Yes
R_3 up 10%	a_1, a_2, a_3	a_3, a_5	a_0, a_3, a_4	a_1, a_3, a_4	a_1, a_5	Yes
R_4 down 20%	$a_0 - a_3$	$a_1 - a_2$	a_2, a_3	a_1, a_2, a_3	a_2, a_3	Yes
R_5 up 15%	a_0, a_5	a_1	a_0, a_2	a_0, a_2, a_3	a_3	Yes
R_6 up 5%	–	a_1, a_2	a_2, a_3, a_5	a_1, a_3	a_1	Yes
R_7 down 10%	a_2, a_4	a_3, a_5	a_0, a_1, a_2	a_1, a_4, a_5	a_2, a_3	Yes
R_8 up 10%	–	a_2	a_0, a_4	a_0, a_2, a_5	a_3, a_4	Yes
R_9 down 5%	–	a_3, a_2	a_1, a_2, a_4	a_2, a_3, a_5	a_1, a_3	Yes
R_{10} up 15%	–	a_1, a_4	a_1, a_3, a_4	a_0, a_1, a_4	a_1, a_2	Yes
R_{11} down 10%	a_0, a_2	a_3, a_4	a_0, a_1	a_1, a_2, a_4	a_1, a_2	Yes
R_{12} down 15%	a_0, a_4	a_1, a_3	a_1, a_2, a_3	a_1, a_2	a_2, a_5	Yes
R_{13} up 5%	–	a_3, a_5	a_1, a_2	a_1, a_2, a_4	a_0, a_2	Yes
R_{14} up 20%	–	a_1, a_3	a_0, a_3, a_4	a_0, a_1, a_2	a_3, a_4	Yes
R_{15} up 5%	–	a_4	a_3, a_5	a_0, a_1, a_3	a_0, a_5	Yes
C_1 down 10%	–	a_4, a_5	a_4, a_5	a_1, a_2, a_3	a_1, a_4	Yes
C_2 up 10%	–	a_2, a_3	a_1, a_2	a_2, a_3, a_4	a_0, a_4	Yes
C_3 down 15%	–	a_1, a_3	a_0, a_1, a_2	a_4, a_5	a_0, a_1	Yes
C_4 down 10%	–	a_0, a_1	a_1, a_2	a_2, a_3	a_2, a_5	Yes
C_5 up 5%	–	a_0, a_1	a_1, a_5	a_1, a_2	a_3, a_4	Yes
C_6 up 15%	–	a_3, a_4	a_1, a_2, a_4	a_3, a_4, a_5	a_1, a_2	Yes
C_7 up 15%	–	a_1, a_4	a_1, a_3, a_4	a_1, a_3, a_5	a_3, a_4	Yes

Table 3.7: Parametric fault fiagnosis with confidence levels of $\approx 98.9\%$ for the elliptic filter.

Injected fault	Diagnosed fault sites at					Deduced fault site
	DC	100Hz	900Hz	1000Hz	1100Hz	
R_1 down 15%	R_1, R_4	R_1	R_1, R_2	R_1, R_2, C_1	R_1, C_1	R_1
R_2 down 5%	R_2	R_2, C_1	R_2, R_3, C_1	R_2, R_3	R_2, C_1	R_2
R_3 up 10%	R_1, R_3	R_3, C_3	R_3, R_4, C_3	R_3	R_3, C_3	R_3
R_4 down 20%	R_1, R_4	R_1, R_4	R_2, R_4, C_1	R_1, R_2, R_4	R_1, R_2, R_4	R_4
R_5 up 15%	R_5	R_5, C_2	R_4, R_5	R_4, R_5, C_2	R_5, R_6, C_3	R_5
R_6 up 5%	–	R_6, C_2	R_6, R_7	R_6, C_2, C_4	R_6, C_2, C_3	R_6
R_7 down 10%	R_3, R_7	R_7, C_3	R_3, R_7	R_3, R_6, R_7	R_3, R_7, C_3	R_7
R_8 up 10%	–	R_6, R_8	R_8, R_9	R_6, R_8	R_8, R_9	R_8
R_9 down 5%	–	R_8, R_9	R_8, R_9	R_9, R_{10}	R_8, R_9	R_9
R_{10} up 15%	–	R_{10}	R_{10}, C_6	R_{10}	R_{10}, C_6	R_{10}
R_{11} down 10%	R_{11}, R_{12}	R_{11}	R_{11}, C_5	R_{11}, R_{12}	R_{11}, R_{12}, C_5	R_{11}
R_{12} down 15%	R_{11}, R_{12}	R_{11}, R_{12}	R_{12}, C_5	R_{12}, C_5	R_{12}, C_5, C_7	R_{12}
R_{13} up 5%	–	R_{13}, C_5	R_{13}, C_7	R_{13}, C_5, C_6	R_{13}, C_5	R_{13}
R_{14} up 20%	–	R_{14}	R_{14}, R_{15}	R_{14}, R_{15}	R_{14}, R_{15}	R_{14}
R_{15} up 5%	–	R_{13}, R_{15}	R_{14}, R_{15}	R_{14}, R_{15}, C_5	R_{14}, R_{15}	R_{15}
C_1 down 10%	–	R_2, C_1	R_2, C_1	R_2, C_1	R_2, C_1	C_1
C_2 up 10%	–	R_5, C_2	C_2, C_4	C_2	C_2	C_2
C_3 down 15%	–	C_3	R_3, C_3	C_3	C_3	C_3
C_4 down 10%	–	R_6, C_4	C_2, C_4	C_2, C_4	C_2, C_4	C_4
C_5 up 5%	–	C_5	R_{12}, C_5	C_5	C_5	C_5
C_6 up 15%	–	R_{10}, C_6	C_6, C_7	C_6, C_7	C_6, C_7	C_6
C_7 up 15%	–	C_6, C_7	C_7	C_6, C_7	C_6, C_7	C_7

Table 3.8: Results of test and diagnosis of some injected faults for LNA.

Circuit Parameter	Coefficients that are out of bounds	Detected	Diagnosed fault sites
R_{bias} down 25%	$a_0 - a_4$	Yes	R_{bias}
L_C down 15%	a_2, a_5	Yes	L_C or C_{C1}
C_{C1} up 10%	a_1, a_2, a_3	Yes	C_{C1} or L_C
L_1 down 25%	$a_0 - a_4$	Yes	L_1
L_2 up 15%	a_0, a_4	Yes	L_2
L_f up 10%	a_1, a_2	Yes	L_f or C_f
C_f up 10%	a_4, a_5	Yes	L_f
C_{C2} down 10%	a_4, a_5	Yes	C_{C2}

Chapter 4

V-Transform Coefficients as Test Signatures

4.1 Introduction

Non-linear circuit testing has been well studied and different methods have been proposed for finding parametric faults [6, 35, 37, 40, 44, 52, 75, 99]. Prominent among them in the industry is the I_{DDQ} based testing where current from the supply rail is monitored and sizable deviation from its quiescent value is reported. However, this requires augmentation of the CUT. For example, in the simplest case a regulator supplying power to any sizable circuit has to be augmented with a current sensing resistor and an ADC (for digital output) and then there is subsequent analysis to be performed on sensed current. Further I_{DDQ} is suitable only for catastrophic faults as the current drawn from the supply is distinguishable only when there is some "big enough" fault so as to change the current drawn from the supply from its quiescent value to a region where it is distinguishable. For example with resistor R_2 being open in Figure 4.1, the current drawn from supply can change by 50% of its quiescent value. Such faults can typically be found by monitoring I_{DDQ} using a current sensor. However parametric deviations say lesser than 10% from its nominal value cannot be observed using this scheme, specially so in the deep submicron era where the leakage currents can be comparable with defect induced current [45]. The other approach for testing parametric faults that can be found in literature [65, 67, 134, 135, 137] is based on the use of neural networks. Neural network based approaches propose the use of circuit observer blocks to track the output for a set of input signals which is used for training the neurons. The trained set of neurons is then used to estimate variations in the output for a standard input stimulus. This method, however, suffers from large amounts of training required and the consequent increase in test application time that the scheme is prohibitive for even medium

sized analog circuits at production. More recently, the use of Volterra series coefficients was proposed to estimate non-linear characteristics of the system. These coefficients are then used for testing the circuit with a pseudo random input stimulus [95, 96]. This method however suffers from the high computational requirement of estimation of Volterra series coeffcients for every circuit at production which can increase the test cost significantly. It is therefore interesting to develop a method to detect parametric faults with little circuit augmentation while keeping the test access mechanism simple and the test application time to a minimum.

To address the issue of parametric deviation, we would typically need more observables to have an idea about the parametric drift in circuit parameters. This would mean an increase in complexity of the sensing circuit. However, we would also want only little augmentation to tap any of the internal circuit nodes or currents. To overcome these seemingly contrasting requirements the method intended should have some way of "seeing through" the circuit with only the outputs and inputs at its disposal. References [53, 93] have accomplished this sort of a strategy for linear circuits in a different context as described next.

Guo and Savir [53] describe a method based on transfer function of a circuit under test (CUT). The transfer function, $H(s)$, of the CUT is expressed as:

$$H(s) = \frac{\sum_{i=0}^{M} a_i s^i}{\sum_{i=0}^{N} b_i s^i} \qquad (M < N) \tag{4.1}$$

Here, a_i and b_i are referred to as transfer function coefficients (TFCs). The CUT is subjected to frequency rich input signals and the output at these frequencies is observed. With these input-output pairs they estimate the TFCs of CUT. These coefficients are now compared with the ideal circuit TFCs, which are known a priori. The CUT is classified faulty if any of the estimated coefficients are beyond the tolerable range. This method necessarily needs the CUT to be linear, as transfer functions are possible only for LTI systems.

To extend the above idea to more general non-linear circuits we adopted a strategy in [122, 125, 126] where we expand the function of the circuit as a polynomial by the Taylor's series expansion about the input voltage mangitude v_{in} at a given frequency, as follows:

$$\begin{aligned} v_{out} = f(v_{in}) = f(0) + \tfrac{f'(0)}{1!}v_{in} + \tfrac{f''(0)}{2!}v_{in}^2 + \tfrac{f'''(0)}{3!}v_{in}^3 + \\ \cdots + \tfrac{f^{(n)}(0)}{n!}v_{in}^n + \cdots \end{aligned} \tag{4.2}$$

where $f(v_{in})$ is a real function of v_{in}. Ignoring the higher order terms in (4.2), we can expand v_{out} up to the n^{th} power of v_{in}, which gives us the approximation in (4.3):

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + \cdots + a_n v_{in}^n \tag{4.3}$$

where $a_0, a_1, a_2, \ldots, a_n$ are all real-valued functions of circuit parameters p_k, $\forall k$. Further assume that normal parameter variations (normal drift) in a good circuit are within a fraction α of their nominal value, where $\alpha << 1$. This means that every parameter p_i is allowed to vary within the range $p_{k,nom}(1-\alpha) < p_k < p_{k,nom}(1+\alpha)$, $\forall k$, where $p_{k,nom}$ is the nominal value of parameter p_k. Whenever one or more of the coefficient values slip outside its individual hypercube we get a different set of coefficients that reflects a detectable fault. Therefore, equation (4.4) describes a hypercube for all parameters that correspond to either good machine values or undetectable parameter faults [35, 53, 99]:

$$a_{i,\min} < a_i < a_{i,\max} \quad \forall a_i,\ 0 \le i \le n \tag{4.4}$$

In the latter portion of this chapter we address an important problem that has kept analog circuit test cost high [86], namely, distinguishing between faults induced due to process variation. For example, we would like to distinguish random drifts in t_{ox}, W, L, and doping densities of devices in an integrated circuits from those resulting from manufacturing defect induced (parametric) faults (e.g., Lithographic errors, etching errors, etc.) that lead to a substantial deviation of a circuit from its nominal behavior but are not large enough to render the circuit dysfunctional. We quantify an error distance measure between faults induced due

to process variation with those induced due to manufacturing defects. We can then estimate the probabilities of a detected fault being caused by process variation or by a manufacturing defect. We make this estimation based on maximizing *a posteriori* probabilities of the two kinds of errors conditioned on the event that a fault is detected.

Most of the material in this chapter is taken from recently published papers [118, 119] by the author. This chapter is organized as follows. Section 4.2 we state previously published results [124] on the polynomial expansion of function $f(v_{in})$ and notions of detectable fault sizes. Section 4.3 outlines V-transform and the resulting sensitivity improvement. In Section 4.4 we describe the problem at hand and discuss the proposed solution with an example. In Section 4.5 we generalize the test solution to an arbitrarily large circuit. Section 4.6 establishes, 1) a method to distinguish between process variation induced faults and those induced due to manufacturing defects and 2) identify the fault site if it is of the latter kind. Section 4.7 presents the simulation results for a standard elliptic filter. We conclude in Section 4.9.

4.2 Background

The coefficients a_i, $\forall 0 \leq i \leq n$, are in general non-linear functions of circuit parameters p_k, $\forall k$. The rationale in using these coefficients as metrics in classifying CUT as faulty or fault free is based on the premise of dependence of coefficients on circuit parameters.

Theorem 4.1 *If coefficient a_i is a monotonic function of all parameters, then a_i takes its limit (maximum and minimum) values when at least one or more of the parameters are at the boundaries of their individual hypercube.*

Lemma 2 *If coefficient a_i is a non-monotonic function of one or more circuit parameters p_i, then a_i can take its limit values anywhere inside the hypercube enclosing the parameters.*

By Theorem 4.1 and Lemma 2 it is clear that by exhaustively searching the space in the hypercube of each parameter we can get the maximum and minimum values of the polynomial

coefficient. Typically this can be formulated as a non-linear optimization problem to find the maximum and minimum values of coefficient with constraints on parameters allowing only a normal drift.

Theorem 4.2 *In polynomial expansion of Non-Linear Analog circuit there exists at least one coefficient that is a monotonic function of all the circuit parameters.*

In conclusion, from Lemma 2 and Theorem 4.2, circuit parameter deviations have a bearing on coefficients and the monotonically varying coefficients can be used to detect parametric faults of the circuit parameters [125].

Definition 3 *A minimum size detectable fault (MSDF), ρ, for a parameter is defined as the minimum fractional deviation of the circuit parameter from its nominal value for it to be detectable with all other parameters held at their nominal values. The fractional deviation can be positive or negative and is named upside-MSDF (UMSDF) or downside-MSDF (DMSDF) accordingly.*

If ψ is the set of all coefficient values spanned by the parameters while varying within their normal drifts, i.e.,

$$\psi = \{\upsilon_0, \upsilon_1, \cdots, \upsilon_n \,|\upsilon_0 \in A_0, \upsilon_1 \in A_1, \cdots, \upsilon_n \in A_n\}$$
$$\forall_k \quad p_{k,nom}(1-\alpha) < p_k < p_{k,nom}(1+\alpha)$$

then by definitions of MSDF, ψ includes all possible values of coefficients that are not detectable. Any parametric fault inducing coefficient value outside the set ψ will result in a detectable fault.

4.3 The V-Transform

We define V-transform coefficients as follows: if $C_1, C_2 \cdots C_n$ are polynomial coefficients of CUT then their V-transform coefficients, $V_{C_1}, V_{C_2} \cdots V_{C_n}$, are

$$V_{C_i} = e^{\gamma C_i'} \ \forall \ 0 \leq i \leq n \tag{4.5}$$

where C_i' are the modified polynomial coefficients defined indirectly as follows

$$\frac{dC_i'}{dp_j} = \left| \frac{dC_i}{dp_j} \right| \ \forall \ 0 \leq i \leq n \tag{4.6}$$

The modification C_i' according to (4.6) ensures that the modified polynomial coefficients are monotonic with the polynomial coefficients. Further, the V-transform coefficients (VTC) are exponential functions of the modified polynomial coefficients and γ is a sensitivity parameter chosen according to the desired sensitivity. The gain in sensitivity of V-transform coefficients to circuit parameters over the sensitivity of ordinary polynomial coefficients is given by

$$\frac{S_{p_i}^{V_{C_i}}}{S_{p_i}^{C_i}} = \frac{\left|\frac{dC_i}{dp_i}\right| \gamma e^{\gamma C_i'} \times \frac{p_i}{e^{\gamma C_i'}}}{\frac{dC_i}{dp_i} \times \frac{p_i}{C_i}} = \gamma C_i \tag{4.7}$$

Choices of $\gamma = 3$, for instance, results in a 3 times more sensitive coefficient to circuit parameters.

4.4 A Problem and an Approach

We shall first illustrate with an example the calculation of limits of the polynomial coefficients for a simple circuit using MOS transistors. We shall follow this up with MSDF values for the circuit parameters.

Example. Two stage amplifier: Consider the cascade amplifier shown in Figure 4.1. The output voltage V_{out} in terms of input voltage results in a fourth degree polynomial:

$$V_{out} = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + a_4 V_{in}^4 \tag{4.8}$$

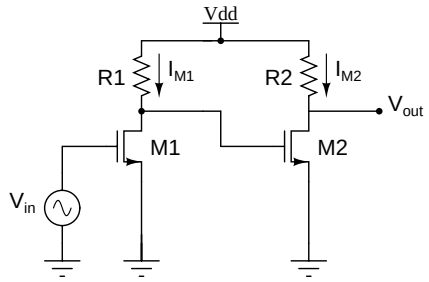


Figure 4.1: Cascade amplifier.

where constants a_0, a_1, a_2, a_3 are defined symbolically in (4.9) for transistors M1 and M2 operating in the saturation region. Nominal values of $V_{DD} = 1.2V$, $V_T = 400mV$, $\left(\frac{W}{L}\right)_{M1} = \frac{1}{2}\left(\frac{W}{L}\right)_{M2} = 20$, and $K = 100\mu A/V^2$ are used for this example.

$$
\begin{aligned}
a_0 &= V_{DD} - R_2 K \left(\tfrac{W}{L}\right)_{M2} \left\{ \begin{array}{l} (V_{DD} - V_T)^2 + R_1^2 K^2 \left(\tfrac{W}{L}\right)^2_{M1} V_T^4 - \\ 2(V_{DD} - V_T) R_1 \left(\tfrac{W}{L}\right)_{M1} V_T^2 \end{array} \right\} \\
a_1 &= R_2 K \left(\tfrac{W}{L}\right)_{M2} \left\{ \; 4R_1^2 K^2 \left(\tfrac{W}{L}\right)^2_{M1} V_T^3 + 2(V_{DD} - V_T) R_1 K \left(\tfrac{W}{L}\right)_{M1} V_T \; \right\} \\
a_2 &= R_2 K \left(\tfrac{W}{L}\right)_{M2} \left\{ \; 2(V_{DD} - V_T) R_1 K \left(\tfrac{W}{L}\right)_{M1} - 6R_1^2 K^2 \left(\tfrac{W}{L}\right)^2_{M1} V_T^2 \; \right\} \\
a_3 &= 4V_T K^3 \left(\tfrac{W}{L}\right)^2_{M1} \left(\tfrac{W}{L}\right)^2_{M2} R_1^2 R_2 \\
a_4 &= -K^3 \left(\tfrac{W}{L}\right)^2_{M1} \left(\tfrac{W}{L}\right)^2_{M2} R_1^2 R_2
\end{aligned}
\tag{4.9}
$$

To find the limit values of the coefficient a_0 we assume that parameters R_1 and R_2 deviate by fractions x and y from their nominal values, respectively. To maximize a_0 we have the objective function (4.10) subject to constraints (4.11) through (4.15). Note that here we have set out to find MSDF of R_1. Similar approach can be used to find the MSDF of R_2.

$$1.2 - R_{2,nom}(1+y)\left\{\begin{array}{l} 2.56\times 10^{-3}+ \\ 1.024\ \times\ 10^{-7}R_{1,nom}^2(1+x)^2 \\ -5.12\ \times\ 10^{-4}R_{1,nom}(1+x) \end{array}\right\} \tag{4.10}$$

$$\begin{aligned} &4.096\ \times\ 10^{-9}R_{1,nom}^2(1+x)^2R_{2,nom}\ (1+y) \\ &+5.12\ \times\ 10^{-6}R_{1,nom}(1+x)R_{2,nom}(1+y) \\ &\quad = 4.096\ \times\ 10^{-9}R_{1,nom}^2(1+\rho)^2R_{2,nom} \\ &\quad + 5.12\quad \times\quad 10^{-6}R_{1,nom}(1+\rho)R_{2,nom} \end{aligned} \tag{4.11}$$

$$\begin{aligned} &1.28\quad \times\quad 10^{-5}R_{1,nom}(1+x)R_{2,nom}(1+y) \\ &-1.536\times 10^{-8}R_{1,nom}^2(1+x)^2R_{2,nom}\ (1+y) \\ &\quad = 1.28\ \times\ 10^{-5}R_{1,nom}(1+\rho)R_{2,nom} \\ &\quad - 1.536\ \times\ 10^{-8}R_{1,nom}^2(1+\rho)^2R_{2,nom} \end{aligned} \tag{4.12}$$

$$\begin{aligned} &2.56\times 10^{-8}R_{1,nom}^2(1+x)^2R_{2,nom}(1+y) \\ &\quad = 2.56\times 10^{-8}R_{1,nom}^2(1+\rho)^2R_{2,nom} \end{aligned} \tag{4.13}$$

$$\begin{aligned} &1.6\times 10^{-8}R_{1,nom}^2(1+x)^2R_{2,nom}(1+y) \\ &\quad = 1.6\times 10^{-8}R_{1,nom}^2(1+\rho)^2R_{2,nom} \end{aligned} \tag{4.14}$$

$$-\alpha \le x, y \le \alpha \tag{4.15}$$

The extreme values for x and y are obained by solving the set of equations 4.10 through 4.15. We get $x = -\alpha$ and $y = -\alpha$ and this gives the MSDF for R_1, as

$$\rho = (1-\alpha)^{1.5} - 1 \approx 1.5\alpha - 0.375\alpha^2 \tag{4.16}$$

Table 4.1 gives the MSDF for R_1 and R_2 based on the above calculation.

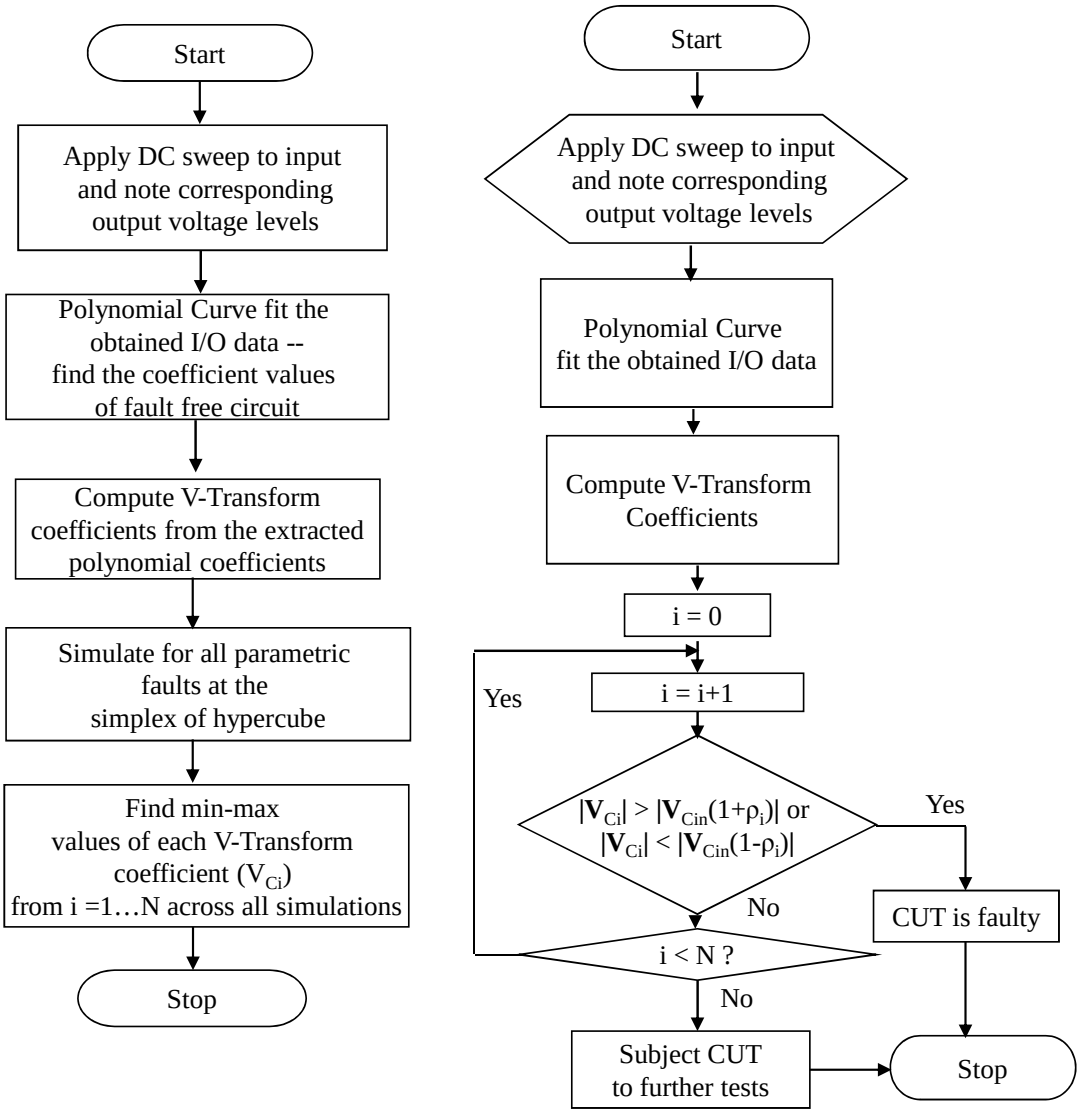
Table 4.1: MSDF for cascade amplifier of Figure 4.1 with $\alpha = 0.05$.

Circuit parameter	%upside MSDF	%downside MSDF
Resistor R_1	10.3	7.4
Resistor R_2	12.3	8.5

4.5 Generalization

The computation of the previous section is too complex for arbitrarily large circuits. Such circuits are handled by first obtaining a nominal numeric polynomial expansion for them. This is done by sweeping the input voltage across all possible values and noting the corresponding output voltages. The output voltage is plotted against the input voltage. A polynomial is fitted to this curve and the coefficients of this polynomial are taken to be the nominal coefficients for the desired polynomial. A V-transform curve is now obtained based on the polynomial curve using the transformation in equation (4.5).

The circuit is simulated for different drifts in the parameter values at equally spaced points from inside the hypercube enclosing each circuit parameter, spaced ϵ apart. Polynomial coefficients and hence V-transform coefficients are obtained for each of these simulations. The maximum and minimum values of coefficient in this search are taken as the limiting values for that coefficient. Once the limiting values for all coefficients have been determined the CUT is subjected to a DC sweep at the input and the output response is curve-fitted using a polynomial of the same order as that used for the fault free circuit. The V-transform coefficients for CUT are now obtained. If there are any coefficients that lay outside the limiting values of the corresponding coefficients of the fault free circuit, we conclude that CUT is faulty. The converse need not be true as there could be other specifications, the circuit needs to meet, which are not captured by polynomial based test. Flowchart I in Figure 4.2 summarizes the process of numerically finding the V-transform coefficients and their bounds. Flowchart II in Figure 4.2 outlines a procedure to test CUT using the V-transform



Flowchart I

Flowchart II

Figure 4.2: Fault simulation process and bounding of coefficients (Flowchart I), and complete test procedure (Flowchart II).

coefficients. The bounds on coefficients of fault free circuit are found a priori as shown in Flowchart I of Figure 4.2.

4.6 Fault Diagnosis

Fault diagnosis involves the location of likely fault sites in a CUT given that the CUT has failed an applied test giving a particular response. We use V-transform coefficients (VTC) to characterize the response of the circuit at different frequencies (about 4 or 5 frequencies are sufficient for most circuits with less than 100 circuit elements), by obtaining its input-output response over the entire input range. Process variation induces a fault-free variation of say σ, about the mean value of every VTC. Any value beyond σ from the mean μ of VTC indicates a circuit failure. Assuming a normal distribution for circuit parameter variation, we can find the probability distribution of the coefficients by Monte-Carlo simulation for process variation of all circuit parameters. Once the Monte-Carlo distributions for the coefficients of fault free circuit are obtained we can inject desired sizes of parametric faults (those that are induced due to manufacturing defects) and obtain the new probability distribution of faulty circuit under process variation.

As an illustration, Figure 4.3 shows the probability density distributions obtained with (broken line) and without (solid line) parametric fault. There are three distinct regions in the probability space of any coefficient C_k. Region R is the fault-free space because coefficients at all frequencies are within the desired limits. Region 1 where dominant mechanism of faults are due to PV of circuit parameters and Region 2 where dominant mechanism of faults is due to manufacturing defects (also called parametric fault). The cross-over point of these two distributions gives the equiprobable region of faults, where we can have faults due to either of the mechanism with the same likelihood. We denote this point on the coefficient axis as $\mathrm{C_{th}}$. Measuring the value of coefficient C of CUT, we can now determine the likelihood of the nature of fault mechanism. That is, $\mathrm{C} \in [\mu, \mathrm{C_{th}}] \implies$ failures due to PV are more in number and $\mathrm{C} \in [\mathrm{C_{th}}, \mu'] \implies$ failures due to parametric faults are more in number. The confidence

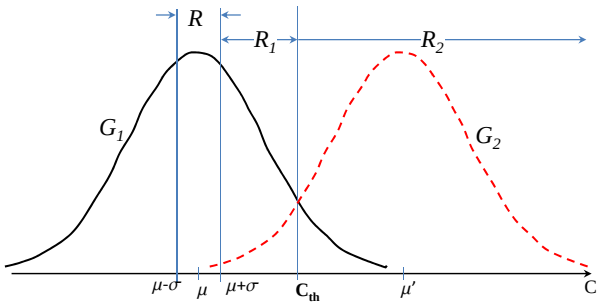


Figure 4.3: Probability distribution of polynomial coefficient C under a parametric fault (broken line) as opposed to that with only process variation (solid line).

of this distinction is given by the relative magnitudes of the two probability density function G_1 and G_2 at the point C on coefficient axis. Once we know, that the fault mechanism is due to a manufacturing defect, we can predict the fault site based on knowledge of the sensitivity of the coefficient to various circuit parameters at different frequencies [128, 129]. A fault dictionary is maintained for faults against circuit parameters at different frequencies. On measuring a parametric fault, the most likely fault site is deduced by intersection of fault sites that can contribute to this fault at most of frequencies. The confidence level (P) of this deduction is given by:

$$P = 1 - \prod_{i=1}^{i=N} (1 - P_i) \tag{4.17}$$

where N is the number of frequencies (including DC) at which the circuit is diagnosed and P_i is the confidence of fault diagnosis at i^{th} frequency.

4.7 Simulation Results

We simulated an elliptic filter shown in Figure 4.4 for V-transform coefficient based test. The circuit parameter values are as in the benchmark circuit maintained by Stroud et al. [70]. Our Monte-Carlo simulation included 50,000 circuit instances, with process variations sampled as zero mean and standard deviation = ±10% of nominal circuit component value. This was repeated for different injected parametric faults to obtain distribution of the coefficients under both parametric faults and process variation (PV) of circuit components.

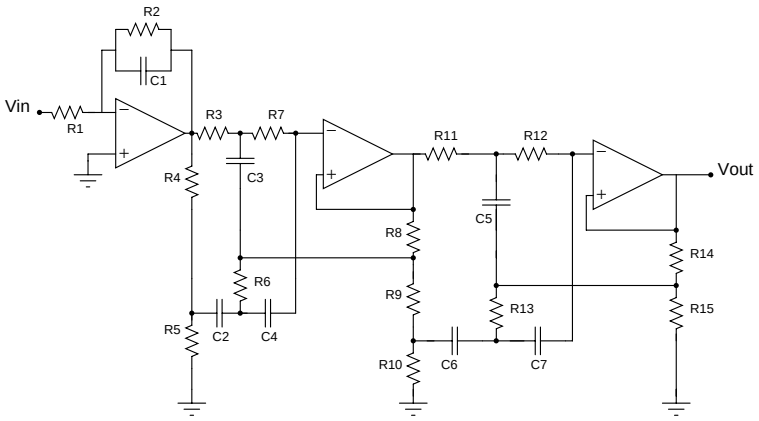


Figure 4.4: Elliptic filter.

Table 4.2: Parameter combinations leading to maximum values of V-transform coefficients with $\alpha = 0.05$ for the elliptic filter.

Circuit Parameter (Ω)	V_{c_0}	V_{c_1}	V_{c_2}	V_{c_3}	V_{c_4}	V_{c_5}
$R_1 = 19.6k$	18.6k	20.5k	20.5k	20.5k	18.6k	18.6k
$R_2 = 196k$	186k	205k	186k	186k	186k	205k
$R_3 = 147k$	139k	154k	154k	154k	139k	154k
$R_4 = 1k$	950	1010	1010	1010	1010	1010
$R_5 = 71.5$	70	80	80	70	80	70
$R_6 = 37.4k$	37.4k	37.4k	37.4k	37.4k	37.4k	37.4k
$R_7 = 154k$	161k	161k	146k	161k	146k	146k
$R_{11} = 110k$	115k	115k	104k	115k	104k	104k
$R_{12} = 110k$	104k	115k	104k	104k	104k	104k

We used parametric faults of sizes $\alpha = 5\%$ from their nominal value to find min-max values of coefficients. Figure 4.5 shows the computed response and the estimated polynomial obtained by curve fitting:

$$\begin{aligned} v_{out} &= 4.5341 - 3.498v_{in} - 2.5487v_{in}^2 \\ &+ 2.1309v_{in}^3 - 0.50514v_{in}^4 + 0.039463v_{in}^5 \end{aligned} \tag{4.18}$$

The combinations of parameter values leading to limits on the coefficients are as shown in Tables 4.2 and 4.3. Some of the circuit parameters are not shown in the table because they do not appear in any of the coefficients and are kept at their nominal values. Further, results on pass/fail detectability of few injected faults are tabulated in Table 4.4. In the cases where

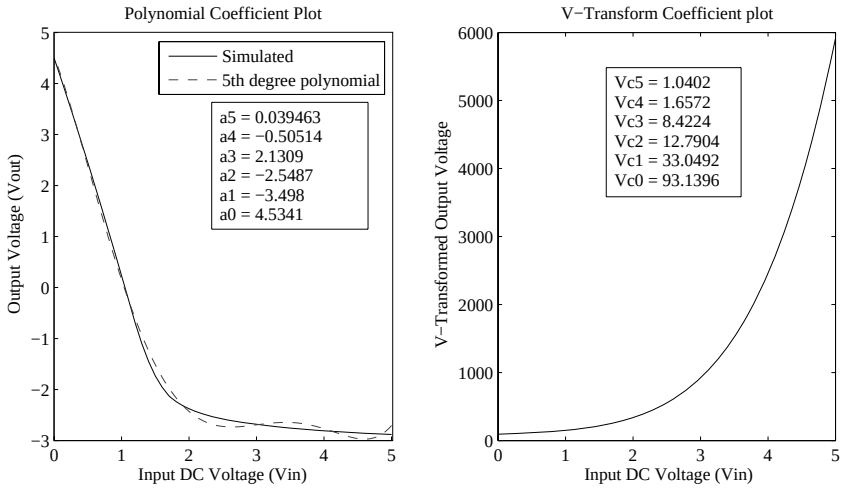


Figure 4.5: DC response of elliptic filter with curve fitting polynomial and V-transform plot.

Table 4.3: Parameter combinations leading to minimum values of V-transform coefficients with $\alpha = 0.05$ for the elliptic filter.

Circuit Parameter (Ω)	V_{c_0}	V_{c_1}	V_{c_2}	V_{c_3}	V_{c_4}	V_{c_5}
R_1 = 19.6k	20.5k	18.6k	18.6k	20.5k	20.5k	20.5k
R_2 = 196k	205k	186k	205k	205k	205k	186k
R_3 = 147k	150k	139k	139k	146k	154k	139k
R_4 = 1k	1010	950	950	950	950	950
R_5 = 71.5	80	70	70	80	70	80
R_6 = 37.4k	39.2k	39.2k	39.2k	39.2k	35.5k	39.2k
R_7 = 154k	146k	146k	161k	146k	161k	161k
R_{11} = 110k	104k	104k	115k	104k	115k	115k
R_{12} = 110k	115k	104k	115k	115k	115k	115k

coefficient deviation lies in the region R_1 for a coefficient C_k, the fault is attributed to PV as opposed to parametric fault. The same procedure is repeated for VTC and the number of cases in which the fault is diagnosed to be in the region R_1 and incorrectly attributed to PV is reduced. This is due to he enhanced sensitivity of V-transform coefficients to circuit parameters. Table 4.5 shows the diagnosed results of a few injected faults using sensitivity of V-transform coefficients to circuit parameters as described in Section 4.6.

Table 4.4: Results for some injected faults in the elliptic filter.

Circuit Parameter	Out of bound polynomial coefficient	Fault detected?	Out of bound V-transform coefficient	Fault detected?
R_1 down 5%	$a_3,\ a_4$	Yes	$V_{c_0} - V_{c_4}$	Yes
R_2 down 10%	a_2	Yes	$V_{c_2},\ V_{c_5}$	Yes
R_3 up 5%	a_3	Yes	$V_{c_1},\ V_{c_2},\ V_{c_3}$	Yes
R_4 down 10%	a_0	Yes	$V_{c_0} - V_{c_4}$	Yes
R_5 up 10%	a_4	Yes	$V_{c_0},\ V_{c_4}$	Yes
R_7 up 5%	None	PV	$V_{c_1},\ V_{c_2}$	Yes
R_{11} up 5%	None	PV	$V_{c_4},\ V_{c_5}$	Yes
R_{12} down 5%	None	PV	$V_{c_4},\ V_{c_5}$	Yes

Table 4.5: Parametric fault diagnosis with confidence levels of $\approx 88\%$ for the elliptic filter.

Injected fault	Diagnosed fault sites					Deduced fault
	DC	100Hz	900Hz	1000Hz	1100Hz	
R_1 dn 15%	R_1 R_4	R_1	R_1, R_2	R_1, R_2 C_1	R_1 C_1	R_1
R_2 dn 10%	R_2	R_2 C_1	R_2, R_3 C_1	R_2, R_3	R_2 C_1	R_2
R_3 up 5%	R_1 R_3	R_3 C_3	R_3, R_4 C_3	R_3	R_3, C_3 C_3	R_3
R_4 dn 20%	R_1 R_4	R_1 R_4	R_2, R_4 C_1	R_1, R_2 R_4	R_1, R_2 R_4	R_4
R_5 up 15%	R_5	R_5 C_2	R_4, R_5	R_4, R_5 C_2	R_5, R_6 C_3	R_5
R_7 dn 10%	R_3 R_7	R_7 C_3	R_3, R_7	R_3, R_6 R_7	R_3, R_7 C_3	R_7

4.8 Experimental Verification

Besides the simulation results presented in the previous section, we carried out an experimental validation of polynomial and V-transform coefficient based scheme for test and diagnosis of parametric faults in the fifth-order elliptic filter that was analyzed in the previous section. For all stimulus application and measurement, we used the National Instruments Educational Laboratory Virtual Instrumentation Suite ELVIS-II$^+$ [3] bench-top module. In the sequel, we will briefly outline the details of the ELVIS II$^+$ bench-top module and our test setup. In Section 4.8.2, we present the measured results.

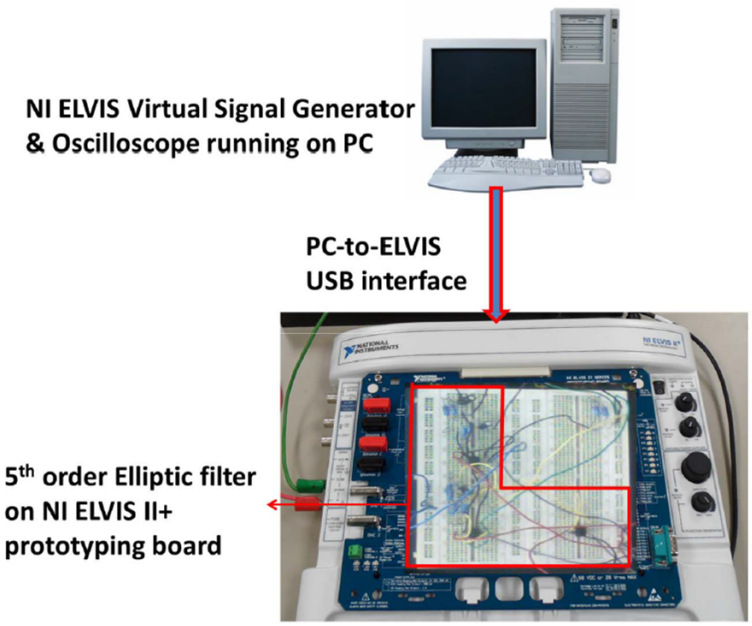


Figure 4.6: Test setup with elliptic filter built on the prototyping board, which is in turn mounted on the NI ELVISII$^+$ bench-top module. Voltage and frequency control of the applied signal is handled through the PC which is connected through USB port to the bench-top module. Output from the circuit is sampled and transferred through the same USB connection to the PC (where it can be post-processed). Also, circuit output can be displayed on the PC using a virtual oscilloscope utility available in the ELVIS software (see Figure 4.7).

4.8.1 Test Setup

The NI ELVIS-II$^+$ system consists of two modules. A *hardware module* comprises of a bench-top module that houses a detachable prototyping board, several power supplies, a function generator, multiple channel digital to analog and analog to digital converters and terminals for oscilloscope and digital multimeter (DMM), all in one portable unit. The second module, a *computer interface* referred to as ELVIS instrument launcher, provides a software interface to control various utilities available on the hardware module.

The experimental set-up for our test scheme is shown in Figure 4.6. The test circuit under test (CUT), a fifth-order elliptic filter, was realized using discrete, off-the-shelf components such as three μA-741 type op-amps, seven electrolytic capacitors, and fifteen carbon coated resistors. These components were mounted on the prototyping board that is housed in

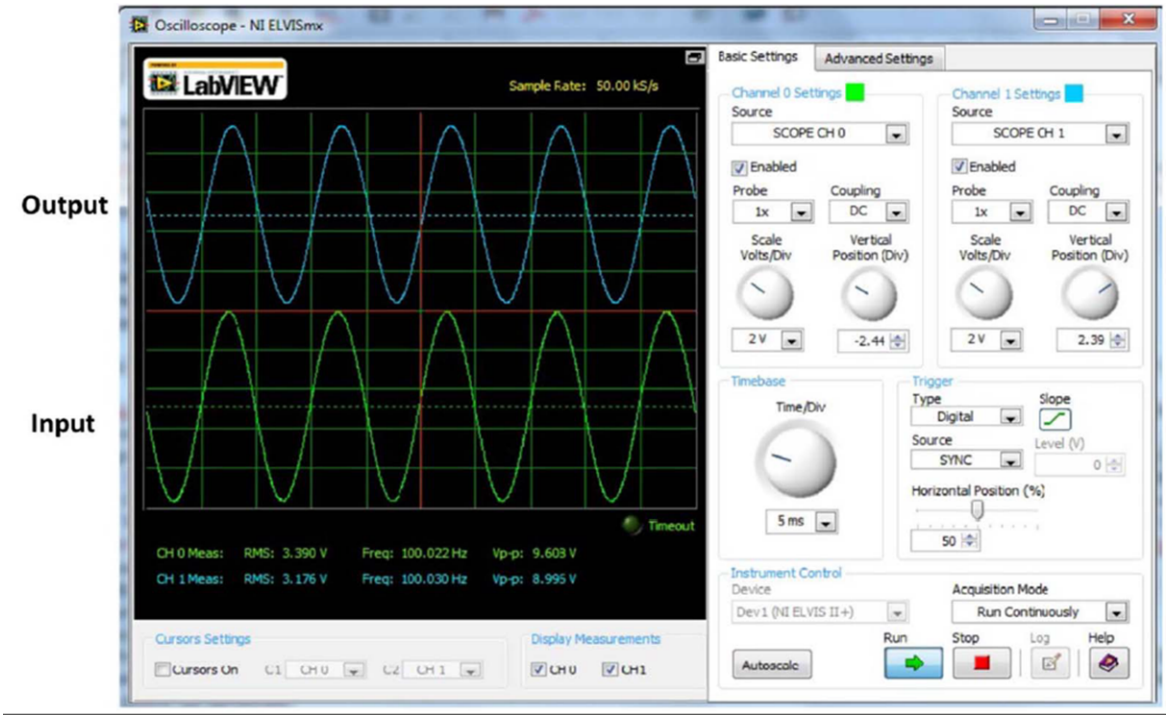


Figure 4.7: Input/output, to/from the elliptic filter displayed on the PC based virtual oscilloscope at a frequency $f = 100$Hz.

the NI ELVIS bench-top module. Inputs can be applied directly from the bench-top module through dedicated pins available on the prototyping board. Frequency and amplitude of the applied inputs can be controlled through a software interface. Thus, a discrete component breadboard implementation in conjunction with virtual instruments for signal generation and response capture gave us the flexibility to inject a variety of parametric faults that might occur in an actual integrated circuit. This allowed us to automate the post-processing analysis of the captured response on the available PC of the system.

4.8.2 Measured Results

Typical input-output waveform pair for the elliptic filter as captured on the PC based ELVIS virtual oscilloscope is shown in Figure 4.7. There are two display channels in the oscilloscope. However, up to eight different inputs can be transferred to the PC, simultaneously, from the ELVIS hardware module. We injected the same set of parametric and

Table 4.6: Measured results for some injected faults in elliptic filter.

Circuit Parameter	Out of bound polynomial coefficient	Fault detection?	Out of bound V-transform coefficient	Fault detection?
R_1 down 5%	a_3	Yes	$V_{c_1} - V_{c_4}$	Yes
R_2 down 10%	a_2	Yes	$V_{c_2},\ V_{c_5}$	Yes
R_3 up 5%	None	No	$V_{c_1},\ V_{c_2},\ V_{c_3}$	Yes
R_4 down 10%	a_0	Yes	$V_{c_0} - V_{c_3}$	Yes
R_5 up 10%	None	No	$V_{c_0},\ V_{c_4}$	Yes
R_7 up 5%	None	No	$V_{c_1},\ V_{c_2}$	Yes
R_{11} up 5%	None	No	$V_{c_4},\ V_{c_5}$	Yes
R_{12} down 5%	None	No	$V_{c_4},\ V_{c_5}$	Yes

catastrophic faults used for the simulated circuit in Section 4.7 (see Tables 4.4 and 4.5). Using V-transform coefficients, all the faults that were identified in the simulation were also detected by measurement. When polynomial coefficients were used without the V-transform, the measurement setup of Figure 4.6 detected fewer faults as recorded in Table 4.6. This reduced performance in fault classification when relying just on polynomial coefficients is due to the measurement noise, whose primary contributor is the ADC-DAC quantization noise from the ELVIS module. We see pronounced reduction in performance when there are fewer than two coefficients that are pushed out of their respective nominal range by the injected parametric fault. However, the increased sensitivity of V-transform coefficients is able to overcompensate for any additional measurement noise and gives the same performance as predicted by simulation.

While there is no loss of test quality with V-transform coefficients, we observe that sometimes coefficients of certain order do not fall out of the nominal range when a fault is introduced. For example, the first fault in Table 4.6, R_1 down 5%, had $V_{c_0} - V_{c_4}$ going out of the nominal range in simulation, but on measurement we see only coefficients $V_{c_1} - V_{c_4}$ falling out of nominal range.

4.9 Sumamrizing V-Transform

In this chapter, a new approach for test and diagnosis of non-linear circuits based on a transformation of polynomial expansion of the circuit was demonstrated. The V-transform renders the polynomial coefficients monotonicity and enhances their sensitivity. The minimum sizes of detectable faults in some of the circuit parameters are as low as 5% which implies that impressive fault coverage can be achieved with V-transform coefficients. The use of V-transform coefficients shows a reduction in masking of parametric faults due to process variation. The method is then extended to sensitivity based fault diagnosis by evaluating V-transform coefficients at different frequencies. The next chapter will examine probability moments of the circuit output as a circuit-test signature, with circuit input as noise (or random variable).

Chapter 5

Probability Moments as Test Signatures

5.1 Introduction

Defects in analog integrated circuits can be classified into two important categories, namely, catastrophic faults (open or shorted components) and parametric faults (fractional deviations of circuit components from their nominal values). While extensive literature [8, 15, 28, 41, 48, 76, 85, 143] exists on test schemes for detecting catastrophic (open/short) faults, testing of parametric faults has not received similar attention [33, 45, 54, 157]. The main reason for this disparity is that catastrophic faults tend to upset the supply current drawn by the circuit or the output voltage by a reasonably large factor and any test scheme based on their observation can conveniently uncover them. Some parametric faults have little impact on supply current and are easily masked by measurement noise or general insensitivity of the output to circuit parameter unless they are tested by careful designed input signal targeting their excitation [111]. Different methods have been proposed to test parametric faults in analog circuits including the use of neural networks [13, 34, 39, 130, 142], spectral analysis [12, 158], transfer function coefficient based testing [53] or, more recently, polynomial coefficient based testing [124, 125]. IDDQ measurement needs a sizable deviation in a circuit component value from its nominal value to be useful [99]. Some test methods require extra die area for testing or call for specific input signal excitation and increased test time [77] (as is the case in neural networks based test methods). While some of these problems are addressed in polynomial based test [124, 125], it is still in its early stages and the correct choices of order and frequency of test points are critical for good fault coverage

Thus, we have a need for a production test, that has little additional hardware, reduced test application time and minimized complexity of input signal design. To respond to the

last question we ask, 'What is the easiest available signal that needs little or no design effort?' Without doubt, it is white noise, always available as random voltage fluctuations across an $R\ \Omega$ resistor due to thermally agitated electrons. Power spectral density of this white noise is given by $\boxed{S_N(f) = 4kTR}$ volt^2/Hz, where k is the Boltzmann constant and T is temperature in Kelvin. Previously [65] white noise has been used as an excitation signal for testing circuits, and the output Fourier spectrum is used for ensuring the circuit conforms to specification. However, in this work, to leverage a random signal like white noise which is characterized only by its statistics such as mean, variance, third and higher order moments, we compute probability moments at the output to be able to derive information on deviation in circuit parameters. Reference [96] proposes the use of a pseudo random noise source as the input and higher order statistics with Volterra kernel at the output as a signature for characterizing the CUT as good or faulty. The work presented in this chapter differs on three counts from previous work, 1) we use a truly random noise source as input, namely, thermal noise from a resistor; though pseudo random noise source will work equally well, 2) higher order moments with an exponentially sensitive random variable transformation is used at the output instead of Volterra kernel. Such a transformation gives better fault resolution for parametric faults than Volterra kernel as shown by our simulation of the elliptic filter example, those results are not included here, 3) we demonstrate fault diagnosis in addition to testing while the earlier work discussed only testing. We view the circuit as a communication channel [9, 115, 116] that transforms the probability density function of the input signal as it propagates through the channel (circuit). The output, which is now the transformed random variable (RV) has its signature moments that are used for testing the CUT for both catastrophic and parametric faults. We show that probability moments can be made exponentially sensitive [119, 127] to circuit parameters, so that parametric faults of 10% and over result in sufficient excursions of the output probability moments to uncover these faults. In the sequel, we describe our scheme on a cascaded amplifier and a low pass filter. We then evaluate the performance of probability moments in conjunction with an

exponential RV transformation to enhance sensitivity for fault detection on a benchmark elliptic filter.

Section 5.2 develops the background on moment theory and random variable transformation, and defines a minimum size detectable fault. The problem at hand and our approach is described with examples in Section 5.3. In Section 5.4, we generalize the method to arbitrarily large circuits. We report experimental results on benchmark elliptic filter in Section 5.5. Section 5.6 introduces fault diagnosis procedure that leverages on unique relationships between moments and circuit components, and Section 5.7 reports results of a fault diagnosis experiment using moments of output of a low noise amplifier. We conclude in Section 5.8.

5.2 Background

We briefly review the moment method to characterize a random variable (RV) (see [120] for more details). We then give a transformation of RV to increase the sensitivity of moments to circuit parameters.

5.2.1 Moment Generating Functions

The j^{th} moment $\forall j = 2 \cdots N$ of a continuous time RV $X(t)$, sampled at time instants $t = kT$, and denoted by X_k where $k = 0, 1 \cdots \infty$ is given by

$$\mu_j = \sum_{k=0}^{\infty} (X_k - \mu_1)^j p(X_k) \tag{5.1}$$

Moment generating function $M(s)$ of such a discrete RV X_k, serves as a convenient expression from which different orders of moments μ_j may be computed using the following relation:

$$\mu_j = \left. \frac{d^j M(s)}{ds^j} \right|_{s=0} \tag{5.2}$$

where $M(s)$ is given by

$$M(s) = E\left(e^{sX_k}\right) = \sum_{k=0}^{\infty} e^{sX_k} p(X_k) \tag{5.3}$$

5.2.2 Random Variable Transformation

We require a random variable transformation [94] that can narrowly track small changes. We look for a transformation with following properties:

1. It increases the sensitivity of output function for small changes in the input.

2. It increases absolute values of the first and higher order moments of the output.

Let X be a RV whose domain is $\mathbb{R}$. We define a transformation $f(X)$ mapping X from $\mathbb{R} \Longrightarrow \mathbb{R}$ as follows:

$$f(X) = Xe^{\alpha X - \frac{\beta}{X}} \tag{5.4}$$

where α, $\beta \geq 0$ are parameters of the transformation. It can be shown that transformation $f(X)$ always gives second and higher order moments which are such that

$$\log_e |\mu_j|_{f(X)} \geq \log_e |\mu_j| \, \forall j = 2, 3, \cdots N \tag{5.5}$$

We plot the first six moments of the transformed RV, with $\alpha = 0.01, \beta = 0.001$ against standard deviation of input RV in 5.1, which shows that the moments of the transformed RV is always greater than that of the RV without transformation. At a few input standard deviations, transformed RV can have significantly higher moments compared to moments without transformation (Notice that the Y-axis in the plots are in the logarithmic scale). This makes the transformation defined in equation 5.4 very amenable for use as a post processing RV transformation at the output of the CUT. Even for small changes in the input, the resulting moments can be significantly different. The sensitivity of the transformed RV to the input RV is given by

$$S_X^f = \frac{X}{f}\frac{\partial f}{\partial X} = 1 + \alpha X + \frac{\beta}{X} \tag{5.6}$$

By appropriate choice of α and β, based on dynamic range of X, we can increase the sensitivity of $f(X)$ for both small and large variations of X.

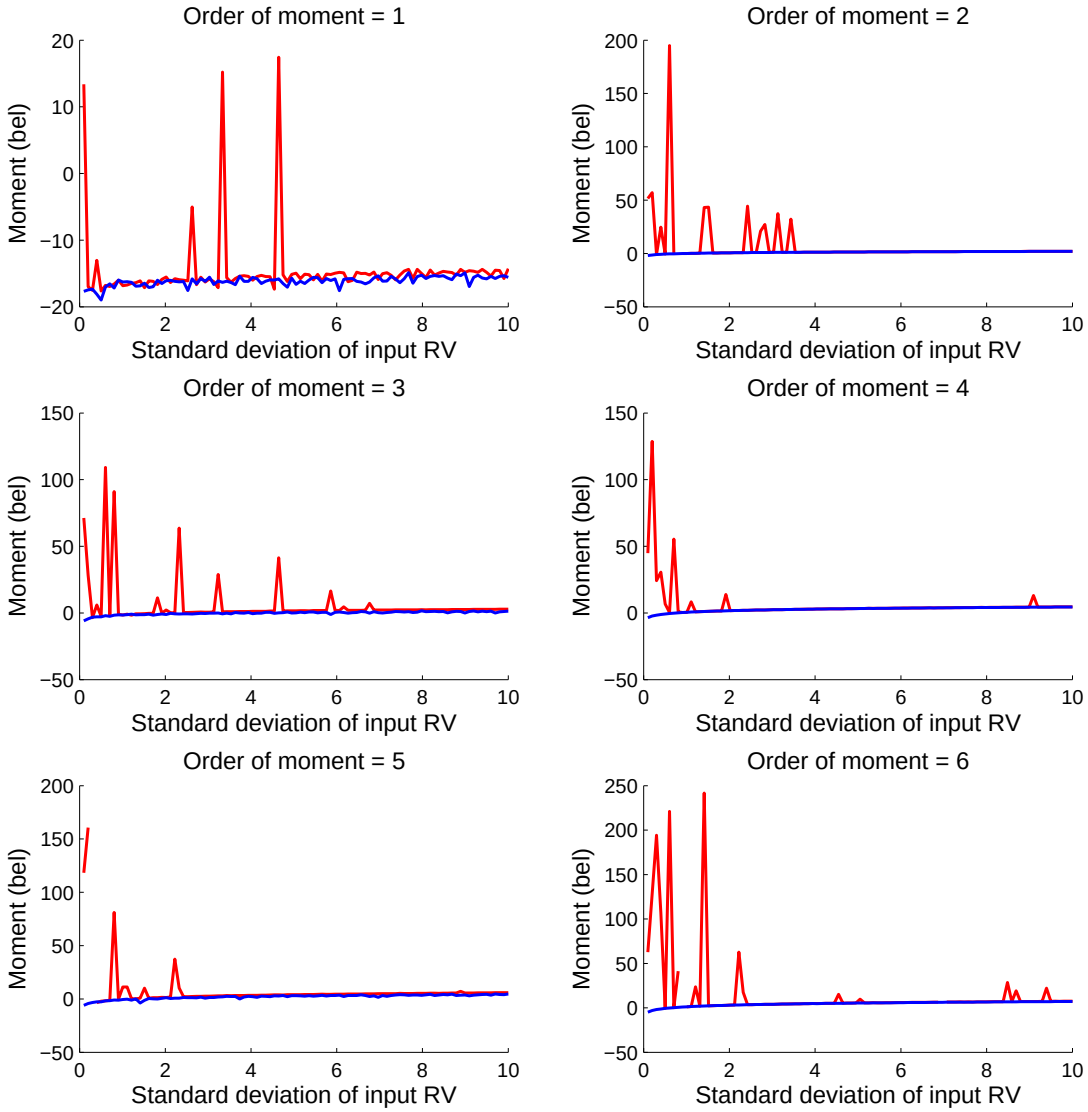


Figure 5.1: Moments of different orders as functions of input noise power (standard deviation of input RV) with (in red/dashed) and without (in blue/solid) RV transformation for first order RC filter. See Figure 5.2.

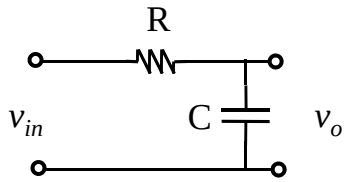


Figure 5.2: First-order RC filter.

5.2.3 Minimum Size Detectable Fault

Definition: Minimum size detectable fault (MSDF) of a circuit parameter is defined as the minimum fractional deviation in the circuit parameter from its nominal value for it to be detectable with all other circuit parameters held at their nominal values. The fractional deviation ρ can be positive or negative and is named upside-MSDF (UMSDF) or downside-MSDF (DMSDF) accordingly. This definition of minimum size detectable fault is general, regardless of the test technique used to uncover faults. In the context of the test technique described here, we define MSDF based on moments of the probability density function of the circuit output. Suppose p_i, where $i = 1 \cdots \mathsf{K}$ is the nominal value of i^{th} circuit parameter with a fault free tolerance range of $p_i\,(1 \pm \gamma)$, and $\overline{\mu_j}$, where $j = 1 \cdots N$ is the j^{th} fault-free probability moment of the circuit output. Then the UMSDF (DMSDF), $\hat{\rho}_i$ ($\check{\rho}_i$) of circuit parameter p_i is given by a minimum value x, such that $p_i\,(1 \pm x)$ puts at least one of the moments $\overline{\mu_j}$ outside the fault free hypersphere $|\overline{\mu_j} - \mu_j| \leq \mu_0$, where μ_0 is the permitted deviation in moments when the circuit parameters are allowed excursions within their tolerance range. As specified earlier, this range is characterized by a tolerance factor γ.

5.3 Problem and Approach

We first illustrate with an example the calculation of limits of the probability moments of a first order low pass filter. We follow this up with calculation of MSDF values of the circuit parameters. We then consider a two stage cascade amplifier.

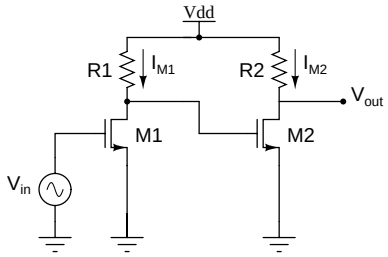


Figure 5.3: A cascade amplifier.

Example 1. First order RC filter: With white noise as the input, the discrete values are sampled Gaussian RV of zero mean and variance, $\sigma_{in}^2 = \frac{N_o}{2}$. The fault-free filtered response has a variance (also the second order moment) $\overline{\mu}_2 = \frac{N_o \pi}{4RC}$. Details of this calculation are shown in the appendix. However, if there is a parametric fault of size x in the circuit parameter R, then the new output variance is given by $\mu_2 = \frac{N_o \pi}{4R(1+x)C}$. If the circuit specifications can tolerate a moment deviation of μ_0, then the MSDF of R is given by the minimum value of x that violates $\overline{\mu}_2 - \mu_2 \leq \mu_0$. For the example in question, since we consider only the second order moment, the MSDF in R, denoted by ρ_R is given by

$$\rho_R = \frac{4\mu_0 CR}{N_o \pi - 4\mu_0 CR} \tag{5.7}$$

Similarly MSDF of capacitor C, ρ_C can be found and by symmetry it is equal to ρ_R.

Example 2. Two stage amplifier: Consider the cascade amplifier shown in Figure 5.3. The output voltage V_{out} in terms of input voltage results in a fourth degree polynomial:

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + a_4 v_{in}^4 \tag{5.8}$$

where constants a_0, a_1, a_2, a_3 are defined symbolically in (5.9) for transistors M1 and M2 operating in the saturation region.

$$
\begin{aligned}
a_0\left(R_1,R_2\right) &= V_{DD}-R_2K\left(\tfrac{W}{L}\right)_2\left\{\begin{array}{l}\left(V_{DD}-V_T\right)^2+\\ R_1^2K^2\left(\tfrac{W}{L}\right)_1^2V_T^4-\\ 2(V_{DD}-V_T)R_1\left(\tfrac{W}{L}\right)_1V_T^2\end{array}\right\}\\
a_1\left(R_1,R_2\right) &= R_2K\left(\tfrac{W}{L}\right)_2\left\{\begin{array}{l}4R_1^2K^2\left(\tfrac{W}{L}\right)_1^2V_T^3\\ +2(V_{DD}-V_T)R_1K\left(\tfrac{W}{L}\right)_1V_T\end{array}\right\}\\
a_2\left(R_1,R_2\right) &= R_2K\left(\tfrac{W}{L}\right)_2\left\{\begin{array}{l}2(V_{DD}-V_T)R_1K\left(\tfrac{W}{L}\right)_1\\ -6R_1^2K^2\left(\tfrac{W}{L}\right)_1^2V_T^2\end{array}\right\}\\
a_3\left(R_1,R_2\right) &= 4V_TK^3\left(\tfrac{W}{L}\right)_1^2\left(\tfrac{W}{L}\right)_2^2R_1^2R_2\\
a_4\left(R_1,R_2\right) &= -K^3\left(\tfrac{W}{L}\right)_1^2\left(\tfrac{W}{L}\right)_2^2R_1^2R_2
\end{aligned}
\tag{5.9}
$$

If the cascade amplifier is excited with white noise at its input, the fault free output can be a estimated as a random variable with its first order moment, namely, mean $\overline{\mu_1}$ given by

$$
\overline{\mu_1} = E\left\{a_0+a_1v_{in}+a_2v_{in}^2+a_3v_{in}^3+a_4v_{in}^4\right\} \tag{5.10}
$$

$$
= a_0+a_1\mu_{1,in}+a_2\mu_{2,in}+a_3\mu_{3,in}+a_4\mu_{4,in} \tag{5.11}
$$

To find MSDF in R_1, let us assume we have a fractional deviation x in R_1 and the other circuit parameters are at their fault free values. If μ_0 is the tolerable fractional deviation in the first order moment at the output, the minimum value of x that satisfies the following inequality is the MSDF of parameter R_1:

$$
\left\{\begin{array}{l}a_0\left(R_1\left(1+x\right),R_2\right)\\ +a_1\left(R_1\left(1+x\right),R_2\right)\mu_{1,in}\\ +a_2\left(R_1\left(1+x\right),R_2\right)\mu_{2,in}\\ +a_3\left(R_1\left(1+x\right),R_2\right)\mu_{3,in}\\ +a_4\left(R_1\left(1+x\right),R_2\right)\mu_{4,in}\end{array}\right\}-\overline{\mu_1}\geq\mu_0 \tag{5.12}
$$

Maximizing x, while meeting the constraint in equation 5.12 gives MSDF of R_1 as

$$
\rho_{\mathrm{R}_1} = \frac{\mu_0}{\mathrm{a}_0+\mathrm{a}_1\mu_{1,\mathrm{in}}+\mathrm{a}_2\mu_{2,\mathrm{in}}+\mathrm{a}_3\mu_{3,\mathrm{in}}+\mathrm{a}_4\mu_{4,\mathrm{in}}} \tag{5.13}
$$

Table 5.1: MSDF for cascade amplifier of Figure 5.3 with $\mu_0 = 0.05$.

Circuit parameter	%upside MSDF	%downside MSDF
Resistor R_1	7	8
Resistor R_2	10.5	7.5

Similarly MSDF of R_2 can be evaluated. Table 5.1 gives the MSDF for R_1 and R_2 based on the above calculation. Nominal values of $V_{DD} = 1.2V$, $V_T = 400mV$, $\left(\frac{W}{L}\right)_1 = \frac{1}{2}\left(\frac{W}{L}\right)_2 = 20$, and $K = 100\mu A/V^2$ are used for this example.

5.4 Generalization

The computation of MSDF in the previous section is too complex for large circuits. As shown in Figure 5.4 a complex circuit having more than 20 components is supplied the input noise voltage (derived from a resistor maintained at desired temperature). The output of the circuit is then passed through a suitable RV transformation function like the one given by equation 5.4. Probability density function (PDF) of the output of this RV transformation is estimated using the histogram spread of the output voltage values. Next, N^{th} order moments (orders up to $N = 6$ are sufficient for most analog circuits having component count of ≤ 40) are found using the moment generating function defined in equation 5.3. The j^{th} derivatives w.r.t. s required for j^{th} order moments are found as finite differences about $s = 0$. Once the fault free values of all N moments are available, single parametric faults are injected into the circuit and the corresponding deviation in one or more moments are noted. Based on the moment deviations that can be tolerated, the fault size injected is steadily increased. The minimum fault size of any circuit parameter that causes at least one of the moments to just fall outside of its tolerance band (also called the fault-free hypersphere) gives the MSDF of that circuit parameter. In Figure 5.5, Flowchart I summarizes the process of numerically finding the probability moments and their bounds and Flowchart II in Figure 5.5 outlines a procedure to test CUT using the PDF moments. The bounds on moments of fault free circuit are found a priori in Flowchart I.

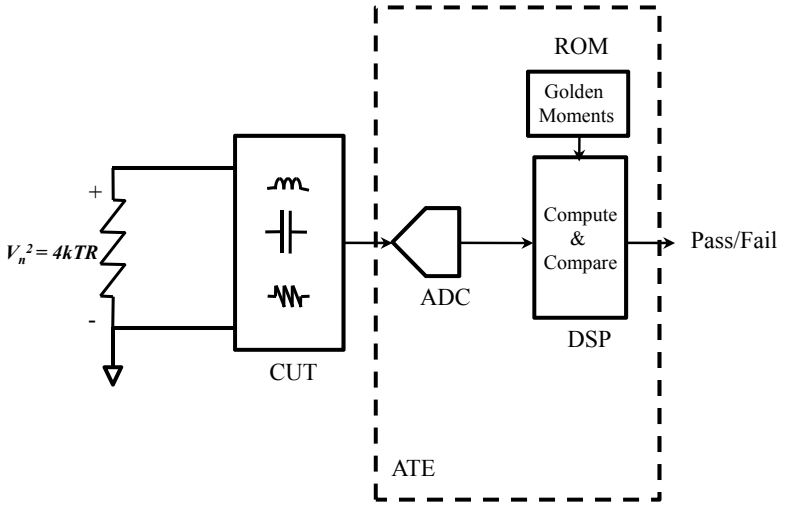


Figure 5.4: Block diagram of a system with CUT using white noise excitation.

5.5 Fault Detection in Elliptic Filter

We simulated an elliptic filter shown in Figure 5.6 according to the test scheme of Figure 5.5. The circuit parameter values are as in the benchmark maintained by Stroud et al. [70]. Thermal noise from resistors R = 40GΩ, 60GΩ, 80GΩ, 100GΩ was used at $T = 300K$. On application of RV transformation, signal levels (and so are moments) significantly better resolved as compared to that without RV transformation. For example, the six fault free moments of the elliptic filter before transformation (for R = 40GΩ) are as follows: $\overline{\mu_1} = 4.53453$, $\overline{\mu_2} = 0.03234$, $\overline{\mu_3} = 0.02345$, $\overline{\mu_4} = 0.01125$, $\overline{\mu_5} = 0.009325$, $\overline{\mu_6} = 0.00623125$. After RV transformation, the fault free moments are given by $\overline{\mu_1} = 338.6453$, $\overline{\mu_2} = 1.8234$, $\overline{\mu_3} = 0.9254$, $\overline{\mu_4} = 0.8812$, $\overline{\mu_5} = 0.6365$, $\overline{\mu_6} = 0.1638125$.

Combinations of parameter values leading to limits on the coefficients are as shown in Tables 5.2 and 5.3. Results on pass/fail detectability of few injected faults are tabulated in Table 5.4.

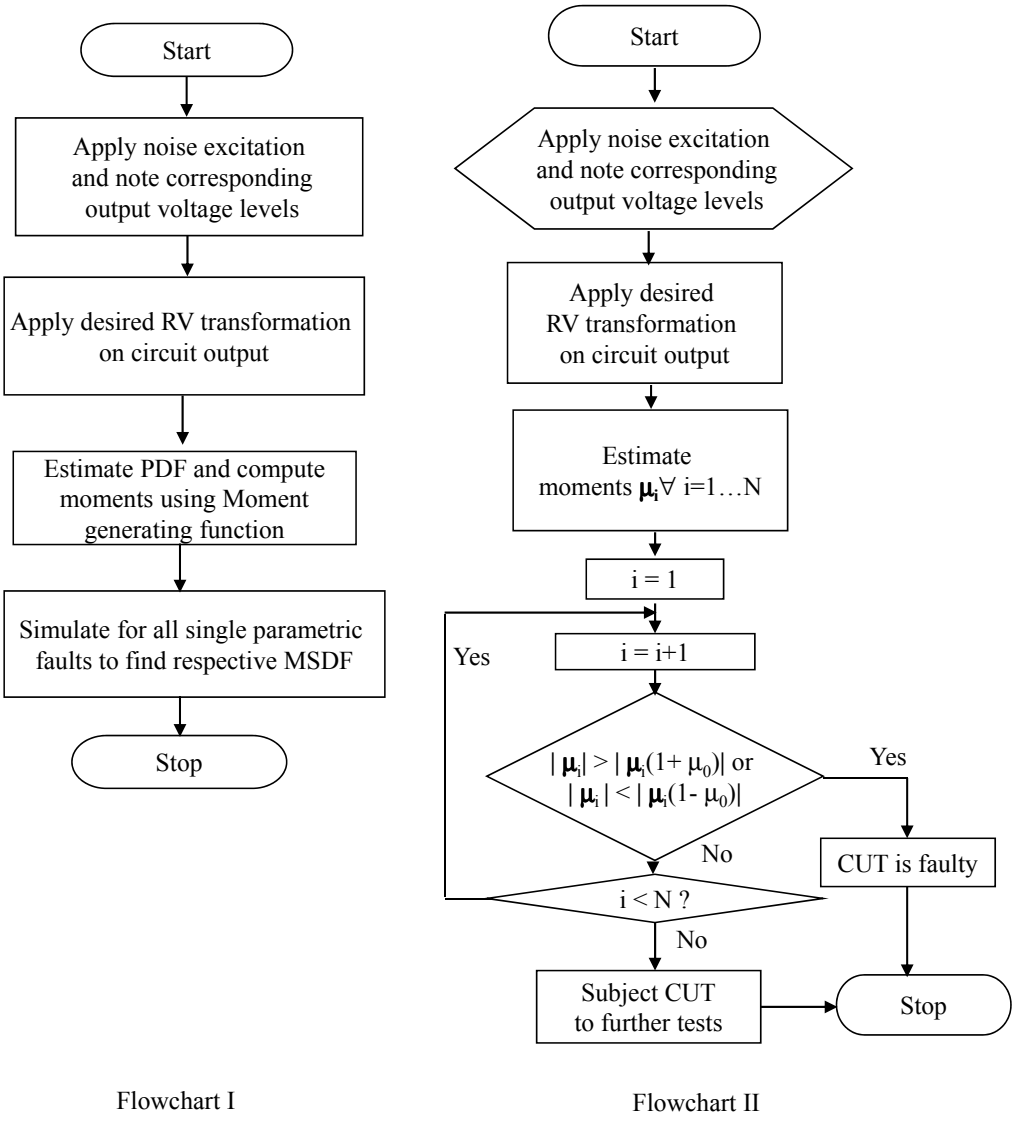


Figure 5.5: Fault simulation process and bounding of moments (Flowchart I), and the complete test procedure (Flowchart II).

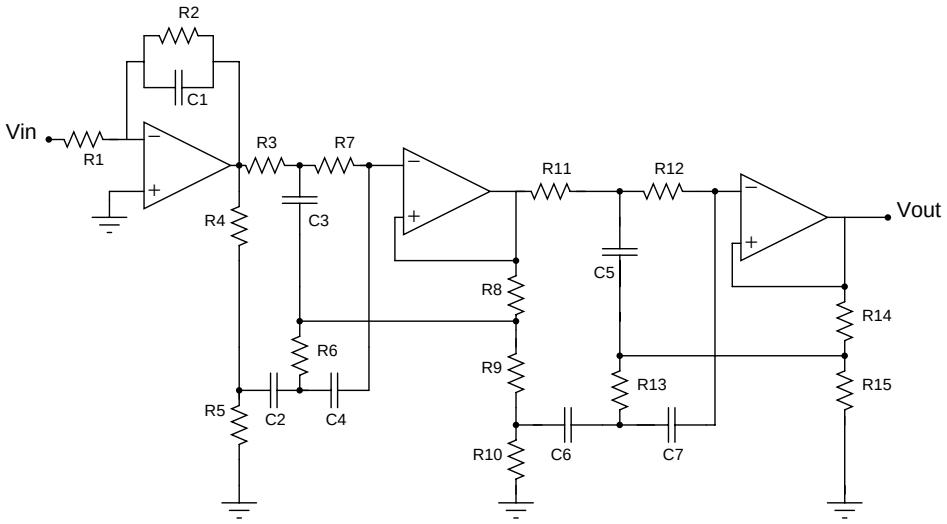


Figure 5.6: Elliptic filter.

5.6 Fault Diagnosis

Flowchart I in Figure 5.7 describes fault simulation and creation of a fault dictionary. Every probability moment of the output is a function of one or more circuit elements. Conversely, we can find one or more moments that are functions of a particular circuit element. By simulating all catastrophic faults in the circuit, we can find those moments that are displaced out of their fault-free ranges for each of the fault and create a fault dictionary. The fault dictionary consists of a list of all catastrophic faults and the corresponding moments that are displaced. Next, using the single catastrophic fault assumption we can compute all the moments of the CUT. Depending on moments that lie outside their fault-free range an estimation of the circuit parameter that has a catastrophic fault is found. Now based on the moments that are displaced from their fault-free value, we can locate the fault in the CUT. Flowchart II in Figure 5.7 gives the diagnosis procedure.

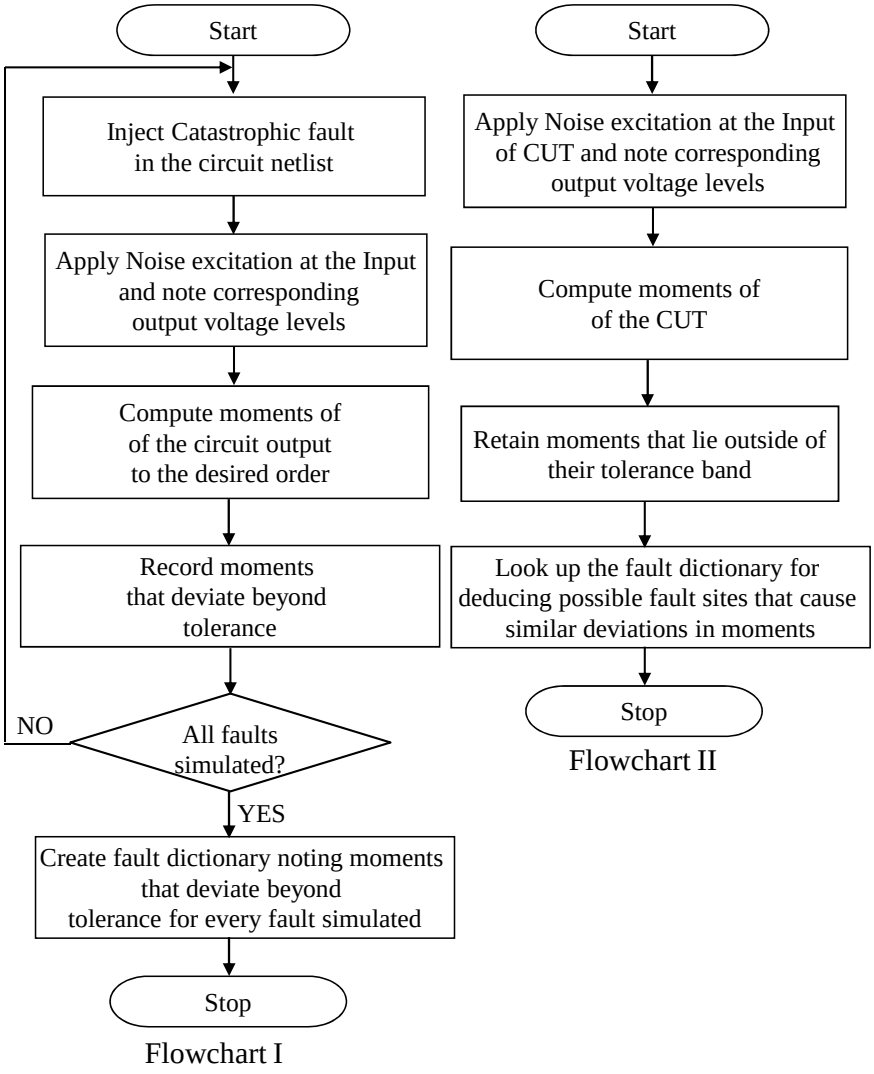


Figure 5.7: Fault simulation (Flowchart I) and Fault diagnosis (Flowchart II) procedures summarized.

Table 5.2: Parameter combinations leading to maximum values of moments with device tolerance $\gamma = 0.05$ in elliptic filter.

Circuit Parameter (Ω, nF)	μ_1	μ_2	μ_3	μ_4	μ_5	μ_6
$R_1 = 19.6$k	19.6k	20.58k	19.6k	20.58k	20.58k	18.62k
$R_2 = 196$k	186.2k	205.8k	205.8k	205.8k	186.2k	186.2k
$R_3 = 147$k	139.65k	147k	139.65k	139.65k	154.35k	147k
$R_4 = 1$k	1050	1050	950	1000	1050	950
$R_5 = 71.5$	75.075	67.925	75.075	71.5	75.075	67.925
$R_6 = 37.4$k	37.4k	37.4k	37.4k	39.27k	39.27k	37.4k
$R_7 = 154$k	154k	154k	154k	146.3k	154k	154k
$R_8 = 260$	260	260	260	260	273	273
$R_9 = 740$	703	777	777	703	777	777
$R_{10} = 500$	500	500	475	475	525	500
$R_{11} = 110$k	115.5k	104.5k	104.5k	104.5k	104.5k	110k
$R_{12} = 110$k	115.5k	104.5k	104.5k	110k	110k	115.5k
$R_{13} = 27.4$k	28.77k	26.03k	26.03k	26.03k	27.4k	26.03k
$R_{14} = 40$	40	40	38	40	40	40
$R_{15} = 960$	912	1008	912	960	912	960
$C_1 = 2.67$	2.8035	2.5365	2.67	2.67	2.67	2.5365
$C_2 = 2.67$	2.8035	2.67	2.8035	2.8035	2.5365	2.67
$C_3 = 2.67$	2.8035	2.8035	2.67	2.5365	2.5365	2.5365
$C_4 = 2.67$	2.8035	2.67	2.5365	2.67	2.5365	2.67
$C_5 = 2.67$	2.8035	2.67	2.8035	2.5365	2.5365	2.67
$C_6 = 2.67$	2.8035	2.5365	2.8035	2.5365	2.67	2.8035
$C_7 = 2.67$	2.67	2.5365	2.8035	2.8035	2.67	2.5365

5.7 Fault Diagnosis in Low Noise Amplifier

We used the low noise amplifier of Figure 5.8 to evaluate our test procedure. The circuit has 16 components. Thus, there are 32 single catastrophic faults corresponding to *opens* and *shorts* of the passive R, L and C elements. For an *open* fault, the element was replaced by a 1GΩ resistance. For a *short* fault, the element was replaced by a 0V voltage source. For the MOS transistor, the *drain* and *source* terminals were short circuited for a *short* and were left open for an *open* fault. For these 32 faults to be uniquely identified, we need at least 5 moments. Each fault causes one or more moments to lie outside its tolerance band. The total number of uniquely identifiable fault cases with N moments $= \Sigma_{n=1}^{N} \binom{N}{n} = 2^N - 1$. Two faults displacing the same set of moments will cause a diagnostic ambiguity. Evaluating

higher order moments, however, gives better diagnostic resolution, which comes at a price of additional computation. Table 5.5 lists faults and the corresponding moments displaced by each fault. We use up to the 6^{th} order moment and observe that out of the 32 faults, only 5 are *not* uniquely diagnosed because they affect identical sets of moments. The number in the last column identifies number of faults displacing the same set of moments. For example, two faults (indicated in the last column) R_{bias}-short and L_c-short displace same set of moments μ_2–μ_6.

5.8 Conclusion

This chapter discussed a new approach for test and diagnosis of non-linear circuits based on probability density moments of the output was presented. We also showed the effective use of RV transformation to sensitize the output moments to circuit parameters. The minimum sizes of detectable faults in some of the circuit parameters are as low as 10% for an elliptic filter, which implies impressive fault coverage can be achieved with moments as a test metric. Further, the prudent choice of RV transformations can enhance the fault detection resolution. We also proposed a method for localizing catastrophic faults and showed that good diagnostic coverages can be obtained by choosing expansions of moments of the order $O(ln(N))$ for N faults.

The next chapter examines the upper bound on defect level and lower bound on fault coverage achievable in signature based test techniques proposed in this chapter and the previous two chapters – namely polynomial coefficients and V-transform coefficients. The approach taken is general enough that bounds derived can be easily extended to any other coefficient-based signature-test schemes.

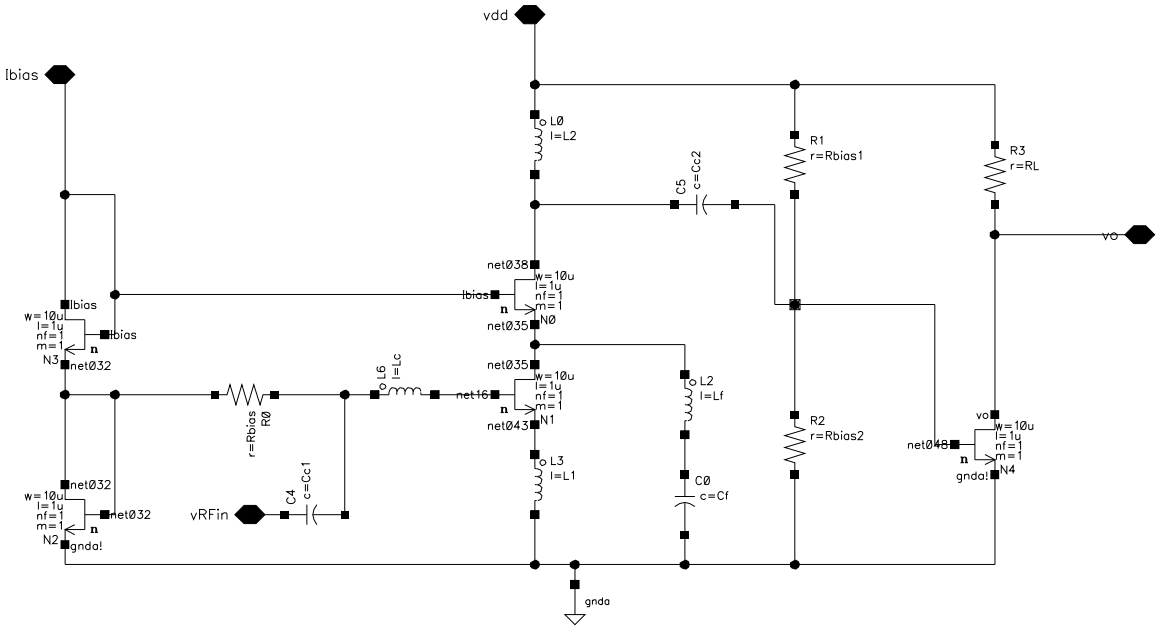


Figure 5.8: Schematic of low noise amplifier.

Table 5.3: Parameter combinations leading to minimum values of moments with device tolerance $\gamma = 0.05$ in elliptic filter.

Circuit Parameter (Ω, nF)	μ_1	μ_2	μ_3	μ_4	μ_5	μ_6
$R_1 = 19.6k$	19.6k	18.62k	19.6k	19.6k	19.6k	20.58k
$R_2 = 196k$	205.8k	205.8k	205.8k	196k	186.2k	205.8k
$R_3 = 147k$	147k	154.35k	154.35k	139.65k	154.35k	154.35k
$R_4 = 1k$	950	1000	1050	950	1050	950
$R_5 = 71.5$	67.925	71.5	75.075	75.075	67.925	71.5
$R_6 = 37.4k$	39.27k	37.4k	35.53k	39.27k	35.53k	35.53k
$R_7 = 154k$	146.3k	161.7k	154k	161.7k	154k	154k
$R_8 = 260$	247	273	247	273	260	247
$R_9 = 740$	703	777	740	777	777	740
$R_{10} = 500$	500	500	475	475	525	475
$R_{11} = 110k$	104.5k	115.5k	115.5k	115.5k	110k	110k
$R_{12} = 110k$	115.5k	110k	115.5k	110k	104.5k	115.5k
$R_{13} = 27.4k$	27.4k	26.03k	27.4k	28.77k	28.77k	26.03k
$R_{14} = 40$	42	40	40	38	40	38
$R_{15} = 960$	1008	960	1008	1008	912	960
$C_1 = 2.67$	2.67	2.5365	2.5365	2.67	2.5365	2.67
$C_2 = 2.67$	2.67	2.67	2.67	2.67	2.67	2.8035
$C_3 = 2.67$	2.8035	2.8035	2.8035	2.8035	2.5365	2.8035
$C_4 = 2.67$	2.8035	2.8035	2.8035	2.8035	2.8035	2.67
$C_5 = 2.67$	2.67	2.8035	2.67	2.8035	2.8035	2.67
$C_6 = 2.67$	2.8035	2.5365	2.8035	2.5365	2.67	2.8035
$C_7 = 2.67$	2.67	2.5365	2.8035	2.67	2.67	2.8035

Table 5.4: Fault detection of some injected faults in elliptic filter.

Circuit Parameter	Out of bound moment	Fault detected?
R_1 down 12%	$\mu_3,\ \mu_1$	Yes
R_2 down 10%	μ_4	Yes
R_3 up 12%	$\mu_1,\ \mu_2$	Yes
R_4 down 10%	μ_2	Yes
R_5 up 10%	μ_4	Yes
R_7 up 15%	$\mu_5,\ \mu_6$	Yes
R_{11} up 15%	μ_3	Yes
R_{12} down 15%	$\mu_2,\ \mu_6$	Yes
C_1 up 11%	$\mu_1,\ \mu_2$	Yes
C_4 up 12%	μ_4	Yes
C_5 down 15%	$\mu_1,\ \mu_6$	Yes

Table 5.5: Fault dictionary for catastrophic faults in low noise amplifier.

Component (ohm, nH, fF)	Nature of fault	μ_1	μ_2	μ_3	μ_4	μ_5	μ_6	Uniquely Diagnosable?
$R_{bias} = 10$	short		✓	✓	✓	✓	✓	No (2)
$L_C = 1$	short		✓	✓	✓	✓	✓	No (2)
$L_1 = 1.5$	short	✓	✓	✓	✓	✓	✓	Yes
$L_2 = 1.5$	short	✓		✓		✓	✓	Yes
$L_f = 1$	short	✓	✓	✓	✓	✓	✓	No (3)
$C_f = 100$	short	✓	✓				✓	Yes
$C_{C2} = 100$	short	✓	✓		✓	✓	✓	Yes
$R_{bias1} = 100k$	short	✓	✓		✓			Yes
$R_{bias2} = 100k$	short	✓					✓	Yes
$R_L = 100k$	short		✓	✓			✓	No (3)
$N_0(D-S)$	short	✓					✓	Yes
$N_1(D-S)$	short		✓		✓			Yes
$N_2(D-S)$	short	✓	✓	✓	✓	✓		Yes
$N_3(D-S)$	short	✓		✓	✓	✓	✓	Yes
$N_4(D-S)$	short					✓	✓	Yes
$R_{bias} = 10$	open	✓	✓	✓				Yes
$L_C = 1$	open	✓	✓					Yes
$L_1 = 1.5$	open			✓		✓	✓	Yes
$L_2 = 1.5$	open	✓	✓		✓		✓	Yes
$L_f = 1$	open	✓		✓			✓	Yes
$C_f = 100$	open	✓				✓	✓	Yes
$C_{C2} = 100$	open						✓	Yes
$R_{bias1} = 100k$	open		✓	✓		✓		Yes
$R_{bias2} = 100k$	open		✓	✓	✓		✓	Yes
$R_L = 100k$	open	✓	✓	✓	✓	✓	✓	No (3)
$N_0(D-S)$	open	✓		✓			✓	Yes
$N_1(D-S)$	open	✓		✓	✓		✓	Yes
$N_2(D-S)$	open					✓		Yes
$N_3(D-S)$	open	✓				✓	✓	Yes
$N_4(D-S)$	open	✓					✓	Yes

Chapter 6

Bounds on Fault Coverage and Defect Level in Signature Based Testing

6.1 Introduction

Faults in analog circuits can be fundamentally divided into two categories, namely, catastrophic and parametric [33]. Catastrophic faults are those in which a circuit component displays extreme deviant behavior from its nominal value. For example, in a resistor such a fault could either be an electrical open or short. Such faults are easy to uncover because they manifest themselves as a sizable deviation in circuit output or performance. On the other hand, component faults are fractional deviations in circuit components from their nominal values. They manifest themselves as subtle deviations in output or performance of the circuit. It is therefore a non-trivial problem to uncover component faults.

Component-based testing of analog circuits has been widely discussed in the literature [16, 37, 53, 92, 93, 100, 111]. Typical methods of characterizing input-output relationship is based on coefficients of transfer function [53], polynomial expansion [124], wavelet transform [23], V-transform [119] or Volterra series [96].

A popular and elegant method was proposed by Savir and Guo [53], in which, analog circuit under test is treated as a linear time invariant (LTI) system. The transfer function (TF) of this LTI system is computed based on the circuit netlist. Note that the coefficients in the numerator and denominator of TF, referred to as transfer function coefficients (TFC), are functions of circuit components. Therefore, any drift in circuit components from their fault free (nominal) values will also result in drifts of the coefficients, as they are linear functions of circuit components. As a result min-max bounds for the coefficients of a healthy circuit are found and these are used to classify the circuit under test (CUT) as good or faulty. Reference [111] shows some limitations of component based analog testing by treating CUT

this way. However, there has been no effort to quantify the achievable fault coverage (FC) and defect level (DL) in TFC based testing of analog circuits. In this work we have derived closed form expressions for upper bound on DL and lower bound on FC.

An approach proposed by Savir and Guo [53] finds component faults by measuring the TFC estimates of the CUT. Minimum size detectable fault (MSDF) in their method is defined as the minimum fault size or minimum fractional drift of the circuit component that will cause the circuit characteristic (in this case the TFC) to lie beyond its permissible limits [53]. In general, computation of MSDF for a circuit component is a non-linear optimization problem and it is computationally expensive to evaluate MSDF for all the circuit components. However, we have some respite in TFCs of linear analog circuit being a linear functions of the circuit components. This implies that TFCs of the circuit take min-max values when at least one of the circuit component is at the edge of its tolerance band (fault free drift range) [53]. This fact is used to avoid solving the non-linear optimization problem. Instead, the circuit is simulated for all combinations of extreme values taken by circuit components in its fault free drift range. The minimum deviation in circuit components causing the coefficients to move out of their min-max bands is thus obtained and is called nearly minimum size detectable fault (NMSDF). The price paid for this simplification is the non-zero difference between NMSDF and MSDF. We quantify this difference and thereby derive bounds for the defect level and Fault coverage achievable through TFC based test methods. Main results of this work have appeared recently [123]. In addition, we present a trade-off between computational overheads of simulation vis-a-vis the effort required to solve the non-linear optimization problem based on the defect level desired.

Most of the ideas in this chapter have been published in a paper [121]. This chapter is organized as follows. In Section 6.2 we formulate the problem. Section 6.3 describes our approach and present analytical proofs for the bounds on DL and FC. Section 6.4 comprises the

simulation results for some well-known circuits. Section 6.5 is a discussion on "simulation–optimization" trade-off based on bounds of defect level and fault coverage. Section 6.6 concludes the chapter.

6.2 Problem Formulation

A linear analog circuit [38, 61, 68] can be represented as a LTI system whose transfer function is given by,

$$H(s) = K\frac{s^{\lambda} + \sum_{k=0}^{\lambda-1} a_k s^k}{s^{\mu} + \sum_{k=0}^{\mu-1} b_k s^k} \qquad (\lambda < \mu) \tag{6.1}$$

Consider a linear analog circuit made up of N circuit components. In the literature, components are often referred to as circuit parameters. However, we will consistently refer to the circuit elements as components. We assume that components have nominal values, $p_{ni},\ \forall i = 1 \ldots N$. In (1), coefficients K, $\{a_k\}$ and $\{b_k\}$ are functions of the circuit components. Let the specified fractional tolerance range for each component be $\pm\alpha$ centered around its nominal value. Thus, the range of values for component p_i is,

$$p_{ni}(1-\alpha) \leq p_i \leq p_{ni}(1+\alpha) \qquad \forall i = 1 \cdots N \tag{6.2}$$

The set of all fault free or undetectable fault values taken by any coefficient a_i in (1) is contained in $[a_{i,min}, a_{i,max}]$. Let C_k be one of the coefficients of the LTI system transfer function in (1). Clearly, C_k is a function of at least one or more circuit components $p_i\ \forall i = 1 \ldots N$. Each coefficient $C_k\ \forall k = 0, \ldots, (\lambda+\mu+1)$ is enclosed in an N-dimensional hypercube spanned by the circuit components. The volume of this hypercube depends on the fault free tolerance range of the circuit components that determine C_k. The extremities of any coefficient C_k of the transfer function occur when at least one component is outside its tolerance range. The circuit is simulated only at the edges of the hypercube. The maximum and minimum values of a coefficient C_k are thus obtained form its bounds.

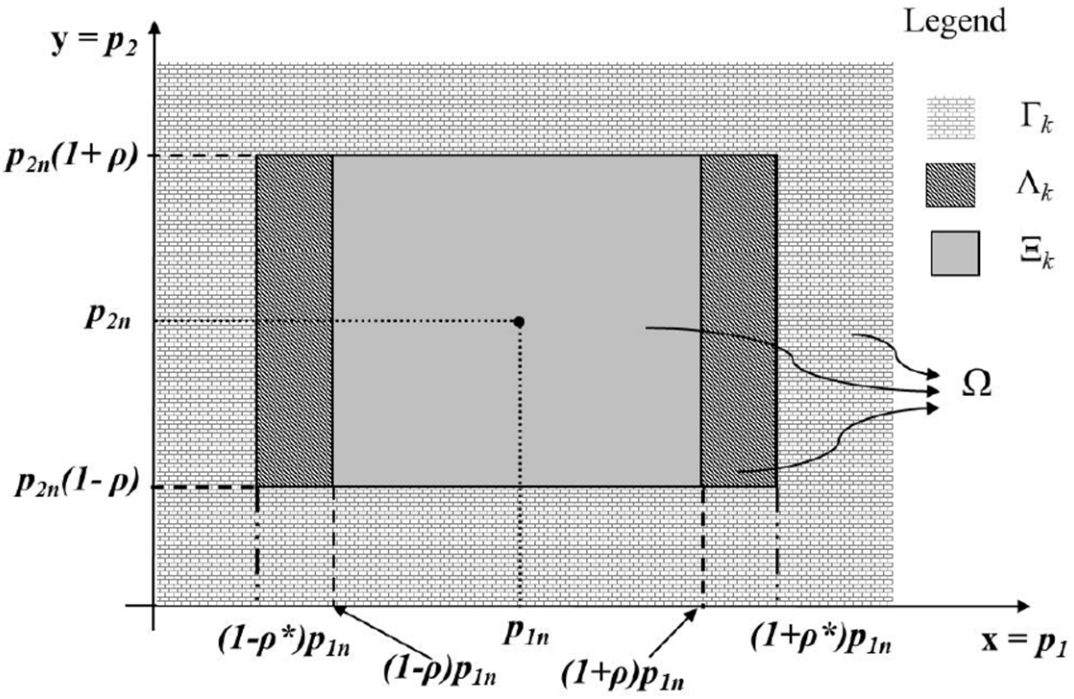


Figure 6.1: Hypercube around coefficient C_k and associated regions.

We formally define the following terms as they are used here.

Definition 1: Minimum size detectable fault (MSDF) of a component p_i is the smallest fractional change ρ_i in its value that makes the circuit faulty when all the other components retain their nominal values.

Definition 2: Nearly minimum size detectable fault (NMSDF) of a component p_i is any small fractional change ρ_i^* in its value that makes the circuit faulty when all other components retain their nominal values. Note that $\rho_i^* \geq \rho_i,\ \forall i = 1 \ldots N$.

Definition 3: Coefficient of uncertainty (ϵ_i) is the assumed difference between the NMSDF and MSDF for the i^{th} circuit component. That is,

$$\epsilon_{\mathrm{i}} = \rho_{\mathrm{i}}^* - \rho_{\mathrm{i}} \tag{6.3}$$

Definition 4: Defect level (DL) of a test procedure is the probability of a faulty circuit passing the test as a fault free circuit.

Definition 5: Fault coverage (FC) of a test procedure is the fraction of all detectable faults that can be detected in CUT by the test procedure.

Consider a TFC C_k being a function of components p_1 and p_2. The hypercube enclosing C_k is shown in Figure 6.1. MSDF values of p_1 and p_2 are found by solving a non-linear optimization problem [53]. The objective for the solution is to maximize (or minimize) C_k with constraint on p_1 and p_2, allowing a drift of $\pm\alpha$ about its nominal value. An example of MSDF calculation has been illustrated by Savir and Guo [53]. NMSDF for p_1 and p_2 are obtained by simulating the circuit at the vertices of the hypercube and measuring the fractional changes in the value of C_k. In general, the MSDF (ρ) and NMSDF (ρ^*) values of a component for drifts above and below its nominal values are not the same. However, for the sake of developing a conservative bound and ease of calculation we consider ρ = Min $(\rho_\uparrow, \rho_\downarrow)$ and ρ^*= Max $(\rho^*_\uparrow, \rho^*_\downarrow)$. Where $\rho_\uparrow$ and $\rho_\downarrow$ denote positive and negative MSDF and $\rho^*_\uparrow$ and $\rho^*_\downarrow$ denote positive and negative NMSDF.

Shaded region Λ in Figure 6.1 is the region of uncertainty and any component drift leading to coefficient lying in this region goes undetected. This region contributes to the defect level DL_{C_k} when the test is based on observing the coefficient C_k.

6.3 Our Approach

6.3.1 Bounding Defect level

The values taken by circuit components can be modeled as independent and identically distributed random variables whose means are the nominal fault-free values and standard deviations (σ) are the tolerance values of circuit components [70].

Two component case

We assume a normal distribution of the components p_1 and p_2 with mean values same as their nominal values (p_{1n} and p_{2n}) and variance σ^2. The defect level from measurement

of coefficient C_k alone is obtained by integrating the joint probability density function of components p_1 and p_2 over the shaded area Λ_k shown in Figure 6.1 and is given by,

$$DL_{C_k} = \int\limits_{\Lambda_k} f_{p1,p2}(x,y)\,dx\,dy \tag{6.4}$$

where $f_{p1,p2}(x,y)$ is the joint probability density function (p.d.f.) of p_1 and p_2 as given by,

$$f_{p1,p2}(x,y) = \frac{1}{2\pi\sigma^2}\exp\left(\frac{-(x-p_{1n})^2}{2\sigma^2} + \frac{-(y-p_{2n})^2}{2\sigma^2}\right) \tag{6.5}$$

We define $Q(x)$ as the integral over the interval $[x,\ \infty)$ of a zero mean and unity variance normal distribution [94]. Similarly, two more integrals, S_1 and S_2, are defined as follows:

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int\limits_{x}^{\infty}\exp\left(\frac{-u^2}{2}\right)du \tag{6.6}$$

$$S_1 = \int\limits_{p_{1n}(1-\alpha)}^{p_{1n}(1+\alpha)}\ \int\limits_{p_{2n}(1-\alpha)}^{p_{2n}(1+\alpha)} f_{p1,p2}(x,y)\,dx\,dy \tag{6.7}$$

$$S_2 = \int\limits_{p_{1n}(1-\alpha)}^{p_{1n}(1+\alpha)}\ \int\limits_{p_{2n}(1-\alpha+\epsilon)}^{p_{2n}(1+\alpha-\epsilon)} f_{p1,p2}\,(x,y)\,dx\,dy \tag{6.8}$$

S_1 and S_2 are evaluated by integrating over the areas shown in Figure 6.1. The Defect Level obtained on observing only a single coefficient C_k is given by,

$$S_1 = \left\{Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right)\right\}^2$$

$$S_2 = \left\{Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right)\right\}\left\{Q\left(\frac{-\alpha+\varepsilon}{\sigma}\right) - Q\left(\frac{\alpha-\varepsilon}{\sigma}\right)\right\}$$

$$DL_{C_k} = S_1 - S_2 \tag{6.9}$$

Generalizing the bound

The result in (9) can be extended to a case where the coefficient C_k depends on all N circuit components. To get an upper bound in this case we take only one component to be at its fault free edge while other components can be anywhere in the fault free band of their values [53]. The maximum defect level from observing C_k alone is given by,

$$DL_{C_k} = \int_{\Lambda_k} \cdots \int f_{p1,p2,\cdots,p_N}(x_1, x_2, \cdots, x_N)\, dx_1 \cdots dx_N \tag{6.10}$$

Theorem 6.1 *For TFCs that are functions of the same circuit components, a component fault (ρ_n) for any $n = 1 \ldots N$, such that $\rho_n \geq \rho$ can escape being detected if and only if it induces all the TFCs into their regions of uncertainty.*

By definition, an undetectable fault corresponds to combinations of TFCs, which are all within their fault free range. A fault is detectable if at least one of the TFCs is beyond its min-max bound, which is obtained on substituting the NMSDF values of circuit components it depends on. This implies a fault can be undetectable only if it induces none of the TFCs beyond its min-max value. That is to say all coefficients are in their regions of uncertainty.

Corollary 1: If κ_i were the event that the i^{th} coefficient is in its region of uncertainty, then the event κ of all coefficients being in their regions of uncertainty is given by

$$\kappa = \bigcap_{i=0}^{\lambda+\mu+1} \kappa_i \tag{6.11}$$

$$\wp(\kappa) = \wp\left(\bigcap_{i=1}^{\lambda+\mu+1} \kappa_i\right) \tag{6.12}$$

$$\Rightarrow \wp(\kappa) \leq \wp(\kappa_i)$$

where $\wp(\kappa)$ denotes probability of event κ. Equation (12) follows from the fact that $\kappa_i \supseteq \kappa$. From (12) and the definition of defect level (DL) as stated in Definition 4, we get

$$DL_{C_k} \geq DL \tag{6.13}$$

From (10), upper bounds on DL_{C_k} and DL are obtained for N circuit components, assuming that each component has an identical coefficient of uncertainty ϵ. We get the following result:

$$\begin{aligned} DL \leq DL_{C_k} \leq & \left\{Q\left(\tfrac{-\alpha}{\sigma}\right) - Q\left(\tfrac{\alpha}{\sigma}\right)\right\}^N \\ & - \left\{Q\left(\tfrac{-\alpha}{\sigma}\right) - Q\left(\tfrac{\alpha}{\sigma}\right)\right\}\left\{Q\left(\tfrac{-\alpha+\epsilon}{\sigma}\right) - Q\left(\tfrac{\alpha-\epsilon}{\sigma}\right)\right\}^{N-1} \end{aligned} \tag{6.14}$$

An analog circuit is typically designed anticipating $\pm\sigma$ variation in its component values [70], where σ is the standard deviation or tolerance of a component about its nominal value and is usually known a priori as a specification of the device. We can therefore assume fault free drifts of $\pm\alpha$ about the nominal value of the circuit component to be equal to $\pm\sigma$ variation in the value of component. Substituting $\pm\alpha = \pm\sigma$ in (14), we get a conservative bound on defect level as,

$$DL \leq 0.8427^N - 0.8427\left\{Q\left(-1+\frac{\epsilon}{\sigma}\right) - Q\left(1+\frac{-\epsilon}{\sigma}\right)\right\}^{N-1} \tag{6.15}$$

6.3.2 Bounding Fault Coverage

Just as we dealt with the problem of bounding the defect level, we shall first consider the two component case and then generalize the result for N components.

Two component case

We assume a normal distribution for each of the components p_1 and p_2 with mean as the nominal value, p_{1n} or p_{2n}, and variance σ^2. We also regard their probability distributions being independent of each other. The Fault coverage achievable by observing coefficient C_k alone is obtained by integrating the joint probability density function of p_1 and p_2 over the

shaded area Γ_k in Figure 6.1. Thus,

$$FC_{C_k} = \int_{\Gamma_k} f_{p1,p2}(x,y)\,dx\,dy \tag{6.16}$$

where region Γ_k is the complement of union of region of uncertainty Λ_k and fault free space Ξ_k of coefficient C_k in quadrant-I in which $p_1, p_2 \in (0,\infty)$. This is the entire region in the quadrant-I denoted as Ω. We can write,

$$\Gamma_k = \Omega \backslash (\Lambda_k \cup \Xi_k) \tag{6.17}$$

$$\mathrm{S}_\Omega = \left\{ Q\left(\frac{-p_{1n}}{\sigma}\right) Q\left(\frac{-p_{2n}}{\sigma}\right) \right\} \tag{6.18}$$

S_Ω in (18) gives probability of the region under Ω. From (17) and (18), we have FC_{C_k} given by (19).

$$\begin{aligned} \mathrm{FC}_{C_k} = &\left\{ Q\left(\tfrac{-p_{1n}}{\sigma}\right) Q\left(\tfrac{-p_{2n}}{\sigma}\right) \right\} \\ &- \left\{ Q\left(\tfrac{-\alpha}{\sigma}\right) - Q\left(\tfrac{\alpha}{\sigma}\right) \right\}^2 \end{aligned} \tag{6.19}$$

In general, nominal value of a component is much greater than its tolerance [70]. We can therefore fairly assume $p_{in} = 5\sigma \,\forall\, i = 1 \ldots N$ and $\pm\alpha = \pm 3\sigma$ in (19) to find FC_{C_k} for two components.

Generalizing the bound

Equation (16) can be extended to N components as in (20).

$$\mathrm{FC}_{C_k} = \int_{\Gamma_k} \cdots \int f_{p1,p2,\cdots,p_N}(x_1, x_2, \cdots, x_N)\,dx_1 \cdots dx_N \tag{6.20}$$

Theorem 6.2 *For TFCs that are functions of the same circuit components, a component fault (ρ_n) for any n=1 ... N such that $\rho_\mathrm{n} \geq \rho^*$ can be detected if and only if it induces at least one of the TFCs beyond their regions of uncertainty.*

By converse of the statement of Theorem 6.1 we have Theorem 6.2.

Corollary 2: If η_i were the event that the i^{th} coefficient is in its region of detectability (Γ_i), then the event η of at least one of the coefficients being in their region of detectability is given by

$$\eta = \bigcup_{i=0}^{\lambda+\mu+1} \eta_i \tag{6.21}$$

Equation (22) follows from (21) as we have $\eta_i \subseteq \eta$.

$$\wp(\eta) \geq \wp(\eta_i) \tag{6.22}$$

By *definition 5* we have $\mathrm{FC}_{C_k} = \wp(\eta_i)$ and $\mathrm{FC} = \wp(\eta)$ therefore on evaluating the integral in (20) we get

$$\mathrm{FC} \geq \mathrm{FC}_{C_k} = \left\{ \prod_{i=1}^{N} Q\left(\frac{-p_{in}}{\sigma}\right) \right\} - \left\{ Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right) \right\}^N \tag{6.23}$$

The result in (23) is a lower bound on fault coverage. On substituting typical values for nominal component, ($p_{in} = 5\sigma$ and $\pm\alpha = \pm\sigma$), we get the following result, which is independent of ϵ:

$$\mathrm{FC} \geq \mathrm{FC}_{C_k} = 1 - 0.8427^N \tag{6.24}$$

6.4 Simulation and Computation

We present plots of defect level in (6.15) against the number of circuit components (N) in Figure 6.2 and against the ratio of coefficient of uncertainty (ϵ) to standard deviation (σ) in Figure 6.3. Figure 6.5 shows the plots of simulated and computed values (from (6.15)) of defect level for different N and $\epsilon = 0.1$ for an RC ladder filter which we will now discuss.

To gain insight, we examined RC ladder filter networks of varying number (n) of RC sections as shown in Figure 6.4. The number of components is $2n$. The transfer function

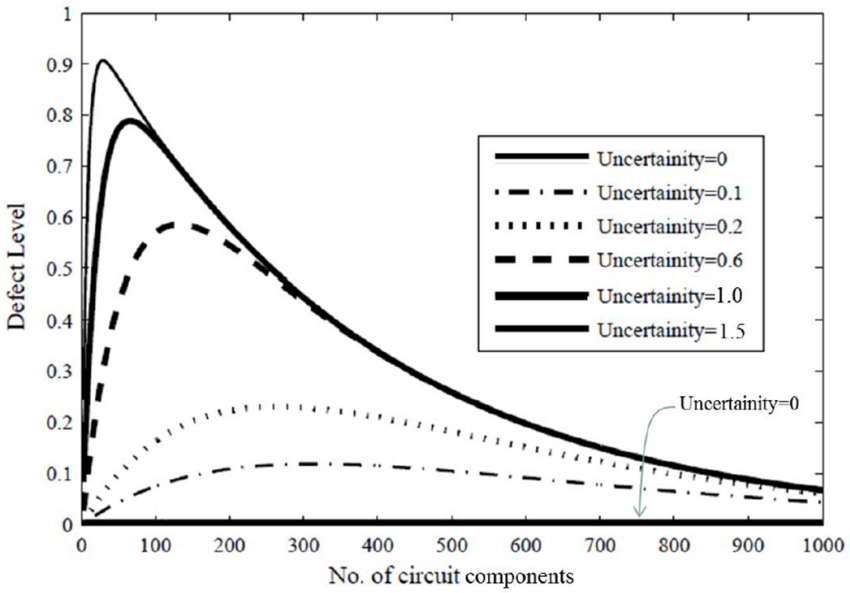


Figure 6.2: Defect level (DL) as a function of number of components (N).

for an RC ladder is readily available in the literature [43, 152]. One of the coefficients of the transfer function was subjected to non-linear optimization [53] to find MSDF for each component. NMSDF for each of the components was found based on the coefficient of uncertainty desired. Here we took $\epsilon = 0.1$ and single component faults were then injected and simulated. The component faults greater than MSDF but lesser than NMSDF which passed the test were then used to find the defect level. Fault coverage was similarly found based on fraction of all the faults that failed the test. It can be seen that there is good coupling between simulated values and theoretically derived bound for both defect level and fault coverage. It is interesting to note the following inferences from the plots in Figures 6.2 and 6.3.

- The defect level initially increases and then decreases with increasing number of components in the circuit. The initial increase can be attributed to the fact that increasing the component count leads to greater probability of fault masking due to departures of component values in opposite directions. This would lead to greater probability of

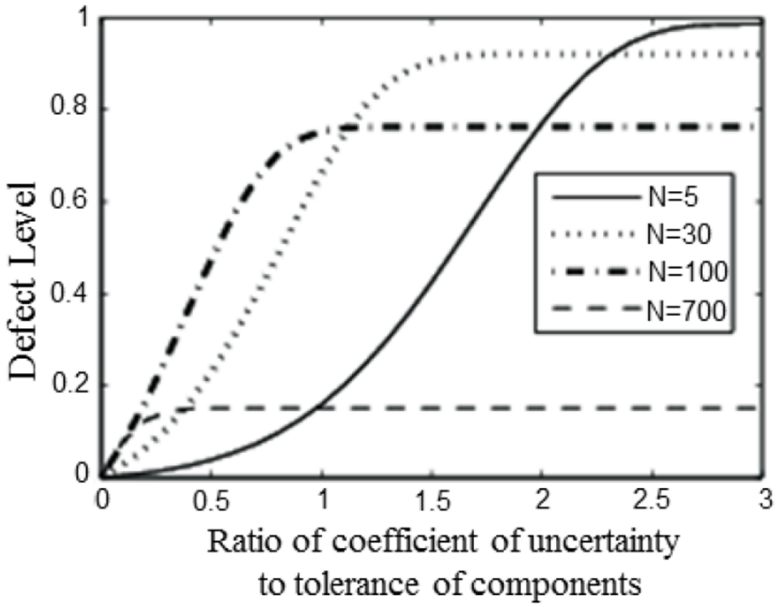


Figure 6.3: Defect level (DL) plotted against ratio of coefficient of uncertainty to tolerance of components ($\frac{\epsilon}{\sigma}$).

fault being masked. However, contrary to intuition, component values beyond a certain threshold result in decrease of defect level. This is a manifestation of stochastic resonance, in that, a circuit with large number of components can aid those sections of circuit that induce faults in opposite directions, thereby resulting in a lower defect level.

- In Figure 6.2, we can see that for medium number of components, defect level is relatively unchanged for larger coefficients of uncertainty. On the contrary ϵ has to be made far smaller to gain in defect level.

- Fault coverage monotonically increases with the number of components as in Figure 6.3. An increase in number of components implies a greater observability for each coefficient. Increased observability is due to the fact that every added component need not increase the count of number of coefficients. For example, a resistor added may not increase the order of the circuit. This leads to more circuit components per coefficient and hence

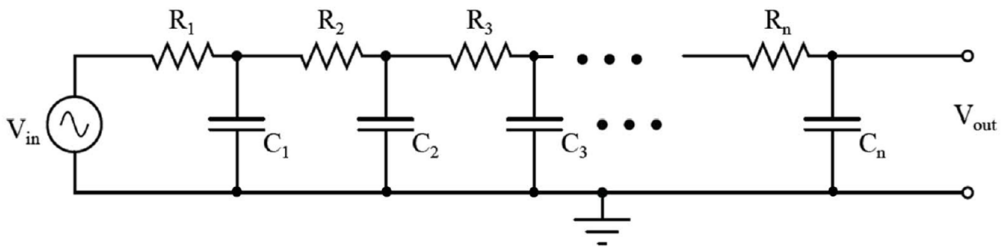


Figure 6.4: RC ladder filter network of n stages.

an increased observability. This in turn increases fault coverage as more components now have a bearing on circuit TFCs.

To further validate the bounds derived, we simulated and tested TFC based approach on benchmark circuits proposed and maintained by Kondagunturi et al. [70]. These are SPICE models from ITC'97 benchmark circuits and Statistical Fault Analyzer (SFA) based models proposed by Epstein et al. [42]. The fault model chosen by us for component faults (soft faults) is σ deviation from nominal value and for catastrophic faults we used open/short faults. To obtain the fault coverage values, we used simulation. Each sample circuit contained a single component fault of size $\pm\sigma, \pm 2\sigma, \cdots, \pm 10\sigma$ (without allowing negative component values), and was simulated to determine whether the fault was uncovered by the TFC based approach for the chosen value of coefficient of uncertainty. We chose $\frac{\epsilon}{\sigma} = 0.1$. The computed and simulated values of defect level and fault coverage for each of the benchmark circuits are tabulated in Table 6.1. In the table, the benchmark with largest component count, ITC'97e, has about 35 components. As a result, we could not verify the tightness of bounds on large component count circuits. To circumvent this predicament, we relied on the RC ladder filter network of Section 6.4. Computed bound and simulated values of defect level as a function of component count are shown in Figure 6.5.

6.5 Simulation Versus Optimization: A Trade-off

We now introduce the "simulation-optimization" tradeoff that results in a typical TFC based analog circuit test scenario. For circuits with more than ten components, the time

Table 6.1: Defect level and fault coverage of benchmark circuits obtained from computation and simulation. For brevity in the table, T: Transistor, O: Opamp, R: Resistor, C: Capacitor, N: Total number of components.

Circuit	Source	Component Count					Defect Level(%)		Fault Coverage(%)	
		T	O	R	C	N	Comp.	Sim.	Comp.	Sim.
Operational Amplifier #1	ITC '97a	8	-	2	1	11	12.51	5.69	84.78	85.31
Continuous-Time State-Variable Filter	ITC '97b	-	3	7	2	12	15.89	5.23	87.17	87.66
Operational Amplifier #2	ITC '97c	10	-	-	1	11	12.51	5.69	84.78	85.31
Leapfrog Filter	ITC '97d	-	6	13	4	23	28	1.33	98.05	98.19
Digital-to-Analog Converter	ITC '97e	16	1	17	1	35	32.62	0.2	99.75	99.78
Differential Amplifier	SFAa	4	-	5	-	9	7.72	6.43	78.57	79.18
Comparator	SFAb	-	1	3	-	4	7.78	3.75	49.57	50.21
Single Stage Amplifier	SFAc	1	-	5	-	6	8.73	6.17	64.19	64.87
Elliptical filter	SFAd	-	3	15	7	25	1.02	0.99	98.61	98.72
Low-Pass Filter	Lucent1	-	1	3	1	5	8.51	5.30	57.50	58.18
RC Ladder Filter (1 stage)	-	-	-	1	1	2	2.5	1.1	55.50	57.33
RC Ladder Filter (18 stage)	-	-	-	18	18	36	30.45	3.98	99.1	99.53
RC Ladder Filter (50 stage)	-	-	-	50	50	100	44.05	11.58	99.7	99.8

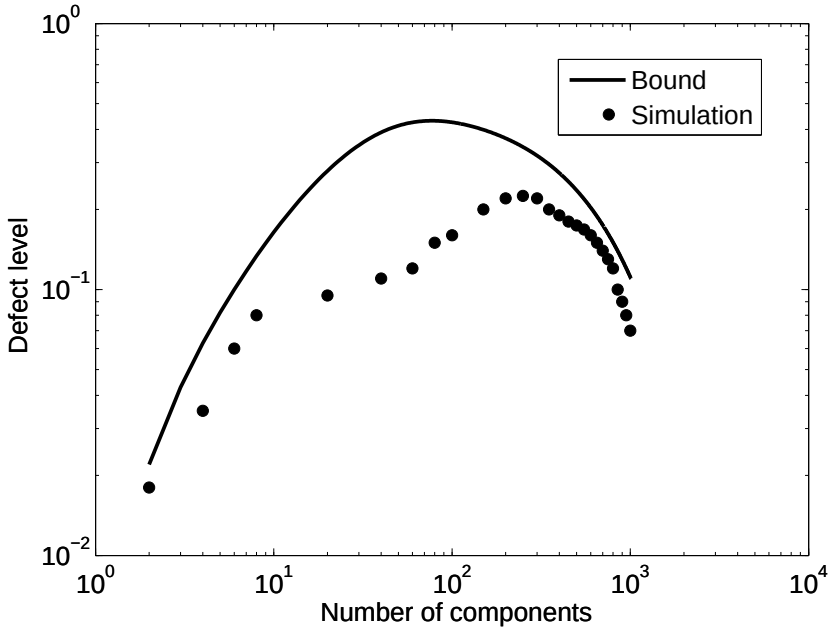


Figure 6.5: Comparison of defect level bounds with simulated value ($\frac{\epsilon}{\sigma} = 0.1$) for RC ladder filter network.

required for simulation is much less compared to optimization of TFC with a coefficient of uncertainty ($\epsilon > 0.1$). However, for smaller component count (e.g., $N = 12$ resistors and capacitors) and uncertainty coefficient ($\epsilon = 0.07$) simulation has to be carried out at a large number of points. The number of points where simulation must be carried out to realize a lower ϵ increases steeply for values of $\epsilon \leq 0.07$ (e.g., points along edges and planes of hypercube enclosing the coefficient instead of just the vertices are now to be simulated) and optimization turns out to be computationally cheaper than simulation. The plot of CPU time required in seconds against uncertainty for both optimization and simulation is plotted in Figure 6.6. The CPU used for simulation in this plot was a Dell machine that has a 2.66 GHz Pentium 4 processor, 1 GB RAM, and 250 GB hard disk space. Note that the time required for optimization remains constant regardless of the value chosen for ϵ, as optimizing results in actual MSDF where $\epsilon = 0$. Time required for simulation decreases exponentially with increasing ϵ. Thus there is a tradeoff between the number of circuit components, coefficient of uncertainty (and in turn defect level) that has to be evaluated before choosing to simulate or optimize a circuit as the computational overheads with wrong choice can be substantial.

6.6 Conclusion

We have derived the bounds for defect level and fault coverage possible in transfer coefficient based analog circuit test. We observe that a higher component count yields lower defect level and higher fault coverage in transfer function coefficient (TFC) based approach for testing linear analog circuits. A possible strategy for deciding whether to use simulation or non-linear optimization [53] to find the bounds on coefficient has been discussed. We find that for lower defect levels it is computationally more expensive to simulate and instead we may use non-linear optimization.

The proposed techniques can be applied to various forms of analog circuit test procedures. In recent publications, we have discussed polynomial coefficient based testing of linear and non-linear circuits [119, 124, 125, 127, 128]. The output function of the circuit is

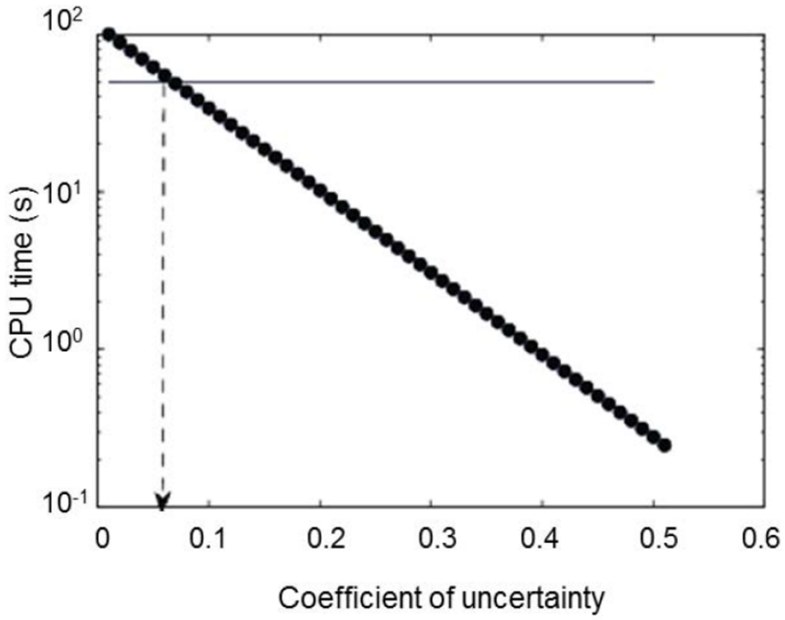


Figure 6.6: CPU time (in seconds) to compute NMSDF by simulation versus coefficient of uncertainty, ϵ.

expressed as a polynomial in the input signal magnitude. Through a proper selection of the test inputs, the coefficients of this polynomial show high sensitivity to component variations. The proposed technique could potentially allow the defect level and fault coverage analysis of non-linear analog circuits.

Chapter 7

Conclusion

Alternate test and fault-model based test methodologies leverage the dependence of outputs of the circuit to the variations in circuit components. In this thesis, we proposed circuit signatures for bolstering both these test methodologies. In particular, we demonstrated parametric and catastrophic fault testing in analog circuits using the proposed signatures. The signatures are based on output's polynomial function approximation for an input stimulus swept across the voltage and frequency range; an exponential transformation of coefficients of the output's polynomial function approximation; probabilistic moments of the output for an random input signal (conforming to a known probability density function). Using the proposed signatures sufficiently small parametric faults of sizes ($\approx$ 5% or more) were uncovered. The proposed signatures have also been used for diagnosis of both catastrophic and parametric faults based on sensitivity analysis of the signatures to the circuit components. Furthermore, the proposed high-sensitivity test signatures increase the correlation of RF/analog circuit outputs to specification of the circuit as is desired in alternate test methodology to minimize yield loss and defect level.

7.1 Thoughts on Future Work

Signatures proposed in this thesis can be used in a closed loop framework such that the correlation of signatures to circuit specifications is further boosted up. Authors in [138] propose an adaptive test methodology for analog circuits in the alternate/signature test framework. Our preliminary studies on this approach have shown the feasibility of this approach with in conjunction with the signatures such as polynomial coefficients and V-transform coefficients proposed in the previous chapters.

7.1.1 Adaptive Test With Signatures

Block diagram in Figure 7.1 shows the high-level conceptual framework of the adaptive test methodology using circuit signatures. The circuit-under-test (CUT) is applied with a carefully crafted stimulus, whose output is then post-processed to generate the signatures such as polynomial coefficients or V-transform coefficients (proposed in previous chapters). The signatures are then used to compute correlation with the actual specification based on actual specification measurement of a small sampling of CUT at run-time. Based on the prevailing correlation, the input stimulus is tuned to achieve optimally sensitive signatures that has the highest degree of correlation to the circuit specification.

7.1.2 Preliminary Experiments

To our knowledge, a run-time, closed-loop tuning of the input stimulus to increase the correlation of the circuit signature to circuit specification for analog circuits has not been attempted before. Our initial experiments on a sample of 400 LNA circuits show promising results on the possibility of using such closed-loop tuning on circuit stimulus to achieve high correlation with specification, which results in lower defect level and yield loss. Figure 7.3 shows the improved correlation between the signature, in this case, V-transform of supply current (I_{dd}), as opposed to just I_{dd} and the specification IIP3 (shown in Figure 7.2). The penalty paid in this process is the extra test-time required to process the signatures and compute the required adjustments to the input stimulus at run-time (for example at production). However, it turns out that even minor adjustments in the input stimulus parameters can give rich dividends in the amount of correlation achieved through such closed-loop tuning. Furthermore, the computation time required for computing the change in stimulus along with the time required to initiate the change in the input stimulus amounts to about 10% increase in the total test-time when compared to test-flows that do not use such closed form tuning. Table 7.1 shows a comparison of three techniques, namely: testing for the specification "as is," using V-transform coefficients in open-loop, and using

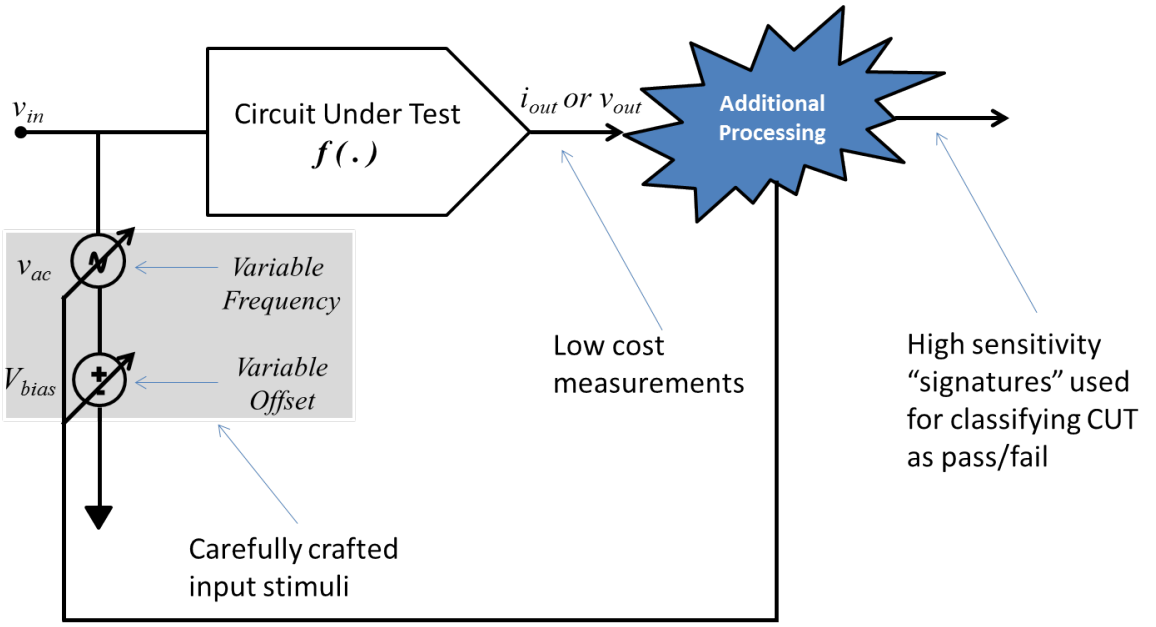


Figure 7.1: Block diagram of the adaptive test system based on circuit signatures.

Table 7.1: Comparison of defect level, yield loss, and test time for actual specification test, signature test in open loop, and signature test in closed loop.

Test Method	Defect Level	Yield Loss	Test Time (per device)
Actual specification test	0%	0%	15s
Signature test in open loop	8%	12%	100ms
Signature test in closed loop	0.8%	1.8%	105ms

V-transform coefficients in closed-loop. Actual specification testing serves as the baseline case (or ideal scenario) for defect level (DL) and yield loss (YL). Notice that signatures taken in open-loop result in a DL and YL of 8% and 12% respectively. Having a closed-loop tuning of the stimulus improves DL and YL to 0.8% and 1.8% with a 5% time-penalty over the open-loop case. But both these techniques give close to a 100x improvement in test-time over the baseline case (of measuring actual specification). More experiments are needed to study how this procedure would scale when the number of CUT are large and any other inadequacies of this approach.

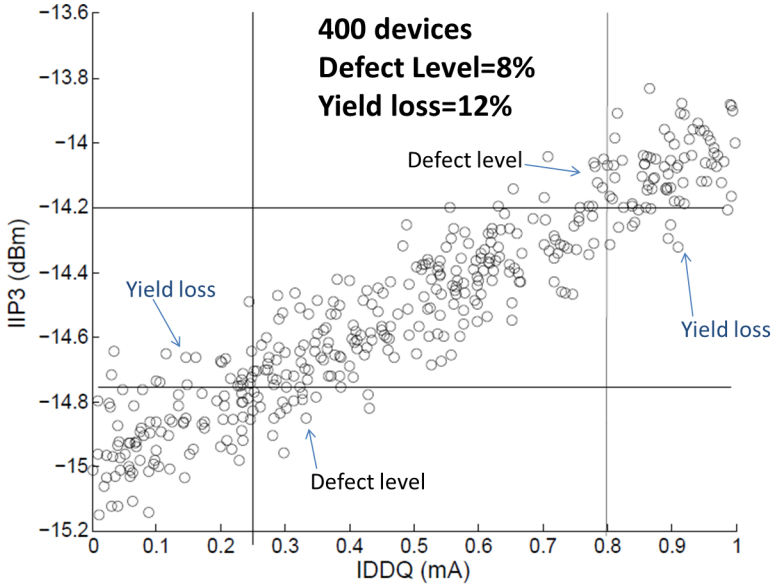


Figure 7.2: Scatter plot of tested devices showing defect level and yield loss for the open loop signature test, where the input stimulus is not tuned adaptively.

7.1.3 Estimating Defect Level in Analog and Radio-Frequency Circuit Testing

The strong correlation between circuit signatures and circuit specifications, and the correlation among circuit specifications themselves can be used to design an optimal set of tests for specifications that will achieve a desired defect level in the tested parts. A small subset of specifications of the circuit that is strongly correlated with the all the specifications, herein referred to as pre-test covers all the specifications to the desired defect level. The goodness of a pre-test (could either be circuit signature or even specification test) can then be characterized as the number of specification tests that it eliminates at a desired defect level. Research along this line is important in making signature based testing relevant and useful in a practical setting like production testing of high-volume integrated circuits in foundries since the biggest concern in adoption of such alternate test strategies is the unknown extent of defect level resulting from eliminating an actual specification test in lieu of signature [136, 26].

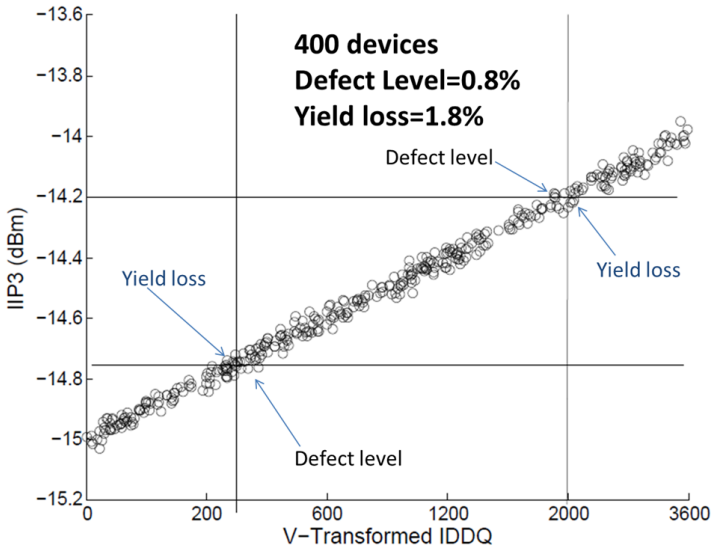


Figure 7.3: Scatter plot of tested devices showing defect level and yield loss for the closed loop signature test, where the input stimulus is tuned adaptively.

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Appendix A

Some Theorems on Nonlinear Systems

Theorem A.1 *If coefficient a_i is a monotonic function of all parameters, then a_i takes its limit (maximum and minimum) values when at least one or more of the parameters are at the boundaries of their individual hypercube.*

PROOF. Let a_i be a function of three parameters say x, y and z. Let a_i reach its maximum value for $(\mathrm{x}_0, \mathrm{y}_0, \mathrm{z}_0)$. Further let $\mathrm{x}_0, \mathrm{y}_0 \neq \alpha$. Now if we can show that the maximum value of the coefficient a_i occurs at $\mathrm{z}_0 = \alpha$ we have proved the theorem. From definition of monotonic dependence of a_i on circuit parameters, (A.1) follows.

$$a_i(\mathrm{x}_0, \mathrm{y}_0, \alpha) \geq \mathrm{a_i}(\mathrm{x}_0, \mathrm{y}_0, \mathrm{z}_0) \ \forall \mathrm{z}_0 \leq \alpha \tag{A.1}$$

As the maximum value taken by $z = \alpha$, it follows that $z_0 = \alpha$. With similar arguments we can show that the minimum value for coefficient occurs when $\mathrm{z}_0 = -\alpha$. Hence the statement of theorem follows.

Theorem A.2 *In polynomial expansion of Non-Linear Analog circuit there exists at least one coefficient that is a monotonic function of all the circuit parameters.*

PROOF. Consider the block diagram in Figure A.1 which models an $2n^{th}$ order Non-Linear analog circuit. x is applied input and y is the response, $a_1 \cdots a_n$ are input summed at each stage. The coefficient corresponding to input x raised to the $2n^{th}$ power is given by G in (A.2).

$$G = \prod_{i=1}^{n} g_i^{2i} \tag{A.2}$$

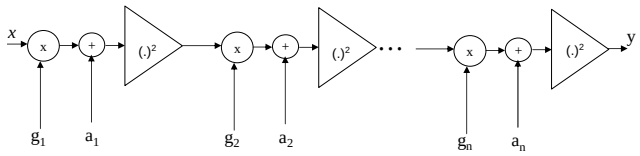

Figure A.1: A possible system model for a non-linear circuit.

where $g_i \; \forall i = 1 \ldots n$ are the monotonic gains of individual stages in the cascaded blocks. As the product of two or more monotonic functions is also monotonic we have G to be a monotonic function. G constitutes the coefficient of the n^{th} power of x in this expansion, as it lies in the main signal flow path from input to output. Thus it is proved that there is at least one monotonically varying coefficient in a polynomial expansion of a non-linear analog circuit. Further, in general the coefficient of $2n^{th}$ power of such a polynomial expansion is monotonic.

Theorem A.3 *A continuous non-monotonic function $f : \Re \rightarrow \Re$ can be decomposed into piecewise monotonic functions of the form:*

$$\begin{aligned} f(x) = f(x)u(x_0 - x) + f(x)\left(u(x - x_0) - u(x - x_1)\right) + \\ f(x)\left(u(x - x_1) - u(x - x_2)\right) + \cdots \\ + f(x)\left(u(x - x_{n-1}) - u(x - x_n)\right) \end{aligned} \tag{A.3}$$

where $x_0, x_1, \cdots x_n$ are all stationary points of $f(x)$ and

$$u(x) = \begin{cases} 1 & \forall\ x \geq 0 \\ 0 & \forall\ x < 0 \end{cases}$$

Proof. By Rolle's theorem [72], if $f : \Re \rightarrow \Re$ is any continuous and differentiable function in the open interval (a, b) and $f(a) = f(b)$, then there exists $c \in (a, b)$ such that $f'(c) = 0$. To extend this result, suppose $f(x)$ is increasing in the interval (a, c^-), that is $f'(x) > 0 \; \forall x \in (a, c^-)$ and decreasing in the interval (c^+, b) that is $f'(x) < 0 \; \forall x \in (c^+, b)$ then at point c, $f'(c) = 0$. In general for a continuous function f over arbitrary interval

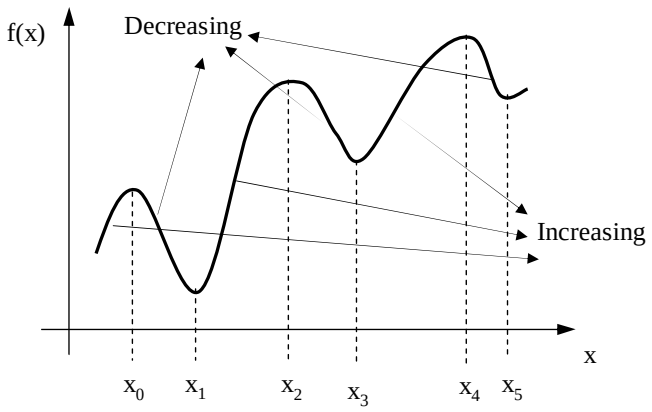

Figure A.2: Non-linear, non-monotonic function decomposed into piecewise monotonic functions.

(α, β) there exists countable number of points x_i such that $f'(x_i) = 0$ as $f(x)$ changes its monotonicity. Now that we have shown x_i are stationary points, it follows that $f(x)$ is monotonic between any two stationary points, i.e., in the interval (x_{i-1}, x_i). The windows generated by the step function $u(x)$ ensures that each term in the summation in (A.3) is monotonic. A typical example is shown in Figure A.2, where f(x) alternates its monotonicity at 6 points namely x_0 through x_5 and at each of these points slope is zero and f'(x)=0. f(x) can be expressed as sum of monotonic functions separated by windows in the intervals $(x_0, x_1), (x_1, x_2), (x_2, x_3), (x_3, x_4), (x_4, x_5)$.

Appendix B

Output Variance of RC Filter

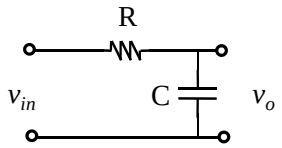

Figure B.1: First order RC low-pass filter.

We use the frequency domain approach to find the transformed RV for Gaussian noise input excitation of a first order RC filter of Figure B.1. The transfer function of that filter is given by

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{sRC+1} \implies |H(j\omega)|^2 = \frac{1}{(\omega RC)^2+1} \tag{B.1}$$

With white noise as the input, the discrete values are sampled Gaussian RV of zero mean and variance $= \frac{N_o}{2}$. The output of this filter which is the filtered response is given by v_o and its frequency domain expression is given by

$$|V_o(j\omega)|^2 = \frac{1}{(\omega RC)^2+1} |V_i(j\omega)|^2 \tag{B.2}$$

To compute the effective second order moment we integrate this output over all frequencies, i.e., $\omega = (0, \infty)$.

$$\begin{aligned} \overline{\mu_2} &= \int_0^\infty \left(\frac{d\omega}{(\omega RC)^2+1} \right) \frac{N_o}{2} \\ &= \frac{1}{RC} \frac{N_o}{2} \arctan(\omega RC)|_0^\infty = \frac{N_o \pi}{4RC} \end{aligned} \tag{B.3}$$